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Optimization and Application of HiPIMS Hafnium Oxynitride (HfO_xN_y) Thin Films in MOS Structures

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This work's main aim was to develop the technology of thin hafnium oxynitride layers employing the High-Impulse Power Magnetron Sputtering (HiPIMS) method with improved electrical parameters. The optimization procedure was implemented using the Taguchi orthogonal tables. During the optimization procedure, the parameters of examined dielectric films were monitored employing optical methods (spectroscopic ellipsometry and refractometry), electrical characterization (C-V and I-V measurements of MOS structures), and structural investigations (AFM, XRD, XPS). The thermal stability of fabricated HfO_xN_y layers up to 800 °C was also examined. The presented results have shown the correctness of the optimization methodology as HfO_xN_y layers formed using optimal HiPIMS process are characterized by improved electrical parameters, which is revealed in lower flat-band voltage (Vfb) values, the disappearance of frequency dispersion of C-V characteristics, reduced effective charge (Qeff/q), and interface traps (Ditmb) densities of examined MOS structures. It is worth underlying that the improved electrical properties can correlate with the lower nitrogen content in the layer bulk and at the semiconductor-dielectric interface. Moreover, the superior stability of HfO_xN_y layers up to 800 °C was proved, and no deterioration of electrical properties or surface morphology has been noticed. However, a slight increase of crystalline phase in the layer bulk was observed. The examinations of HfO_xN_y layers revealed comparable electrical properties and higher immunity to thermal treatment of dielectric films formed using HiPIMS compared to the standard Pulsed Magnetron Sputtering technique. Finally, we successfully applied HiPIMS HfO_xN_y films as gate dielectric films in MOSFET devices. The fabricated structures revealed improved electrical properties compared to FET structures based on silicon dioxide (SiO_2) gate dielectric layers.

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Warsaw University of Technology
Faculty of Electronics and Information Technologies
Institute of Microelectronics and Optoelectronics

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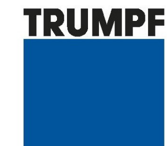
Acknowledgments

- Mirosław Puźniak



TRUMPF Hüttinger
generating confidence

- Wojtek Gajewski

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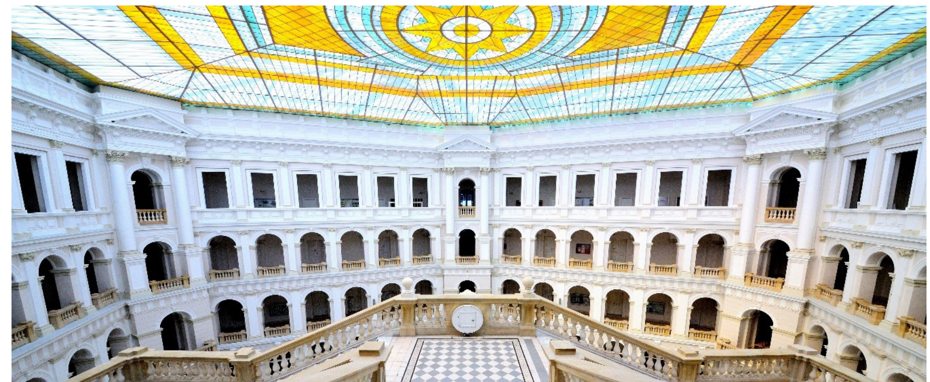
- Marcin Żelechowski

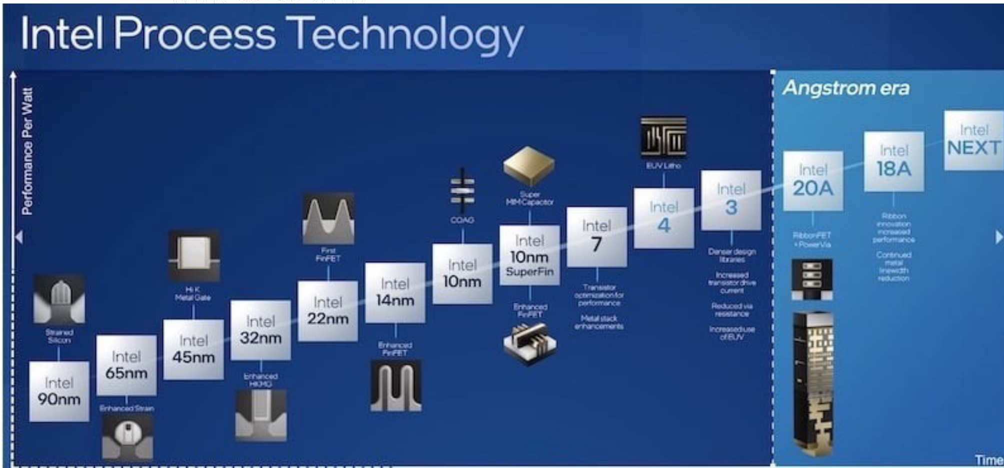


Warsaw University of Technology (PL)

Agenda

- Introduction + motivation
- Taguchi orthogonal tables approach
- Experimental
- Results
- Conclusion

Introduction



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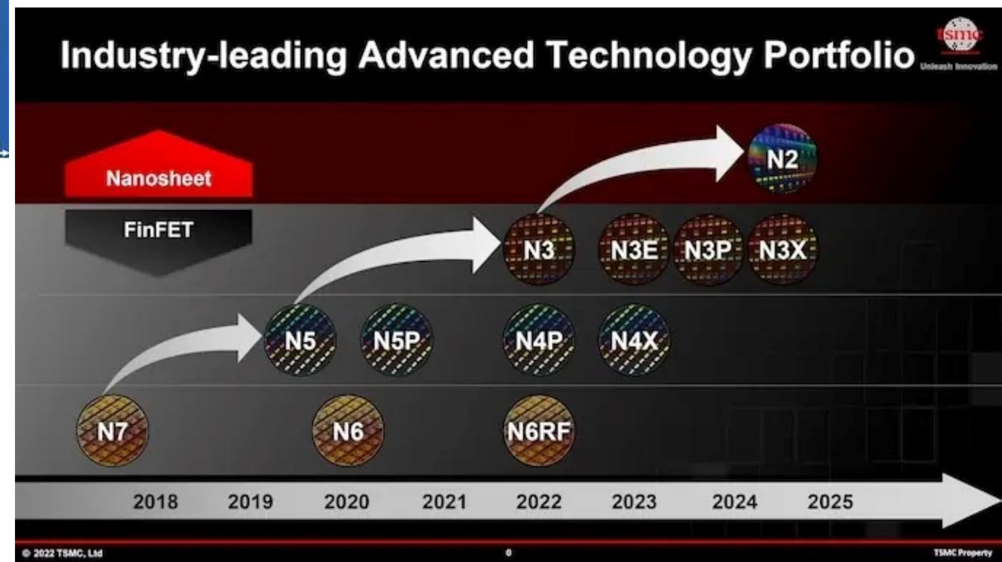
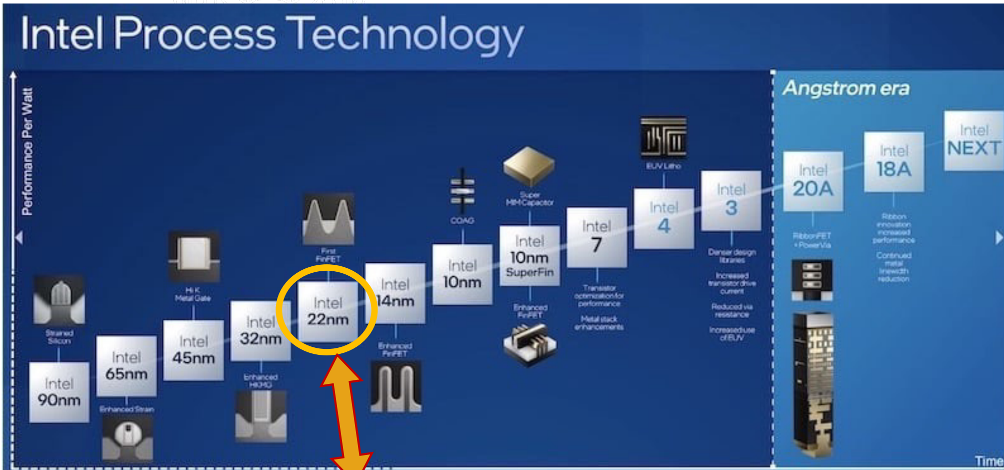


Introduction



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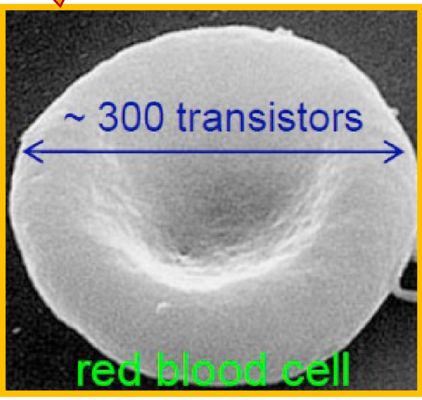

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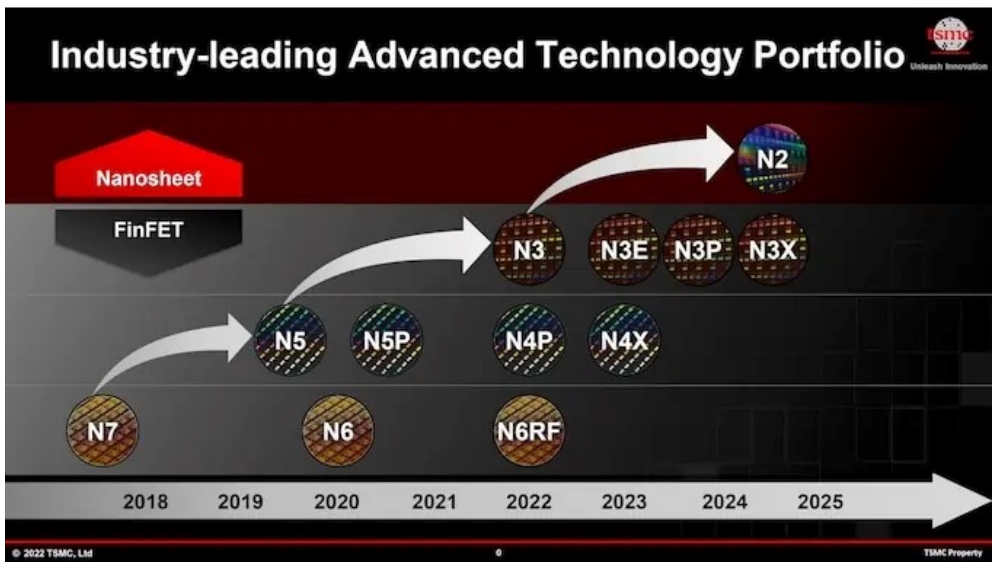


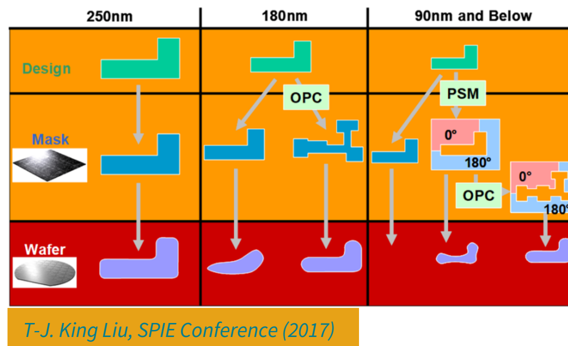
Introduction

Novel materials
- high-k dielectrics
- metal gates (different for P/N FETs)
- silicides
- low-dimensional materials
- epitaxial layers

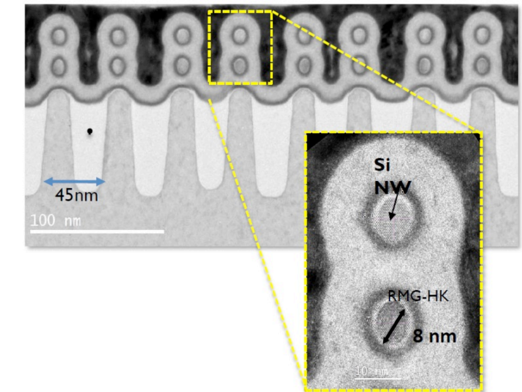
Novel architectures
- FinFETs
- GAA
- UTBB SOI / SON
- Nanosheet / forksheet

Novel technologies / tools
- Strain engineering
- ALD / ALE
- EUV / EUV hNA
- tilted implantation (TII)
- multi patterning

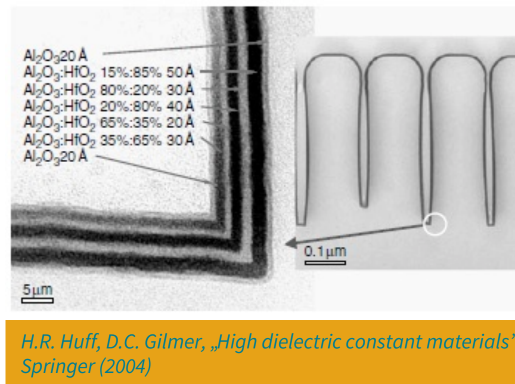
New design / layout considerations



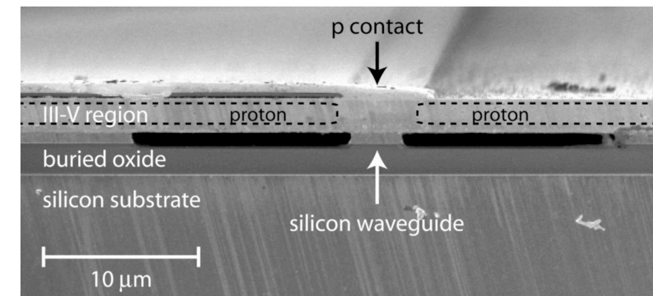
T-J. King Liu, SPIE Conference (2017)



H. Mertens, IMEC VLSI (2016)



H.R. Huff, D.C. Gilmer, „High dielectric constant materials" Springer (2004)



J. Bowers et al., IEEE Custom ICs Conf (2013)

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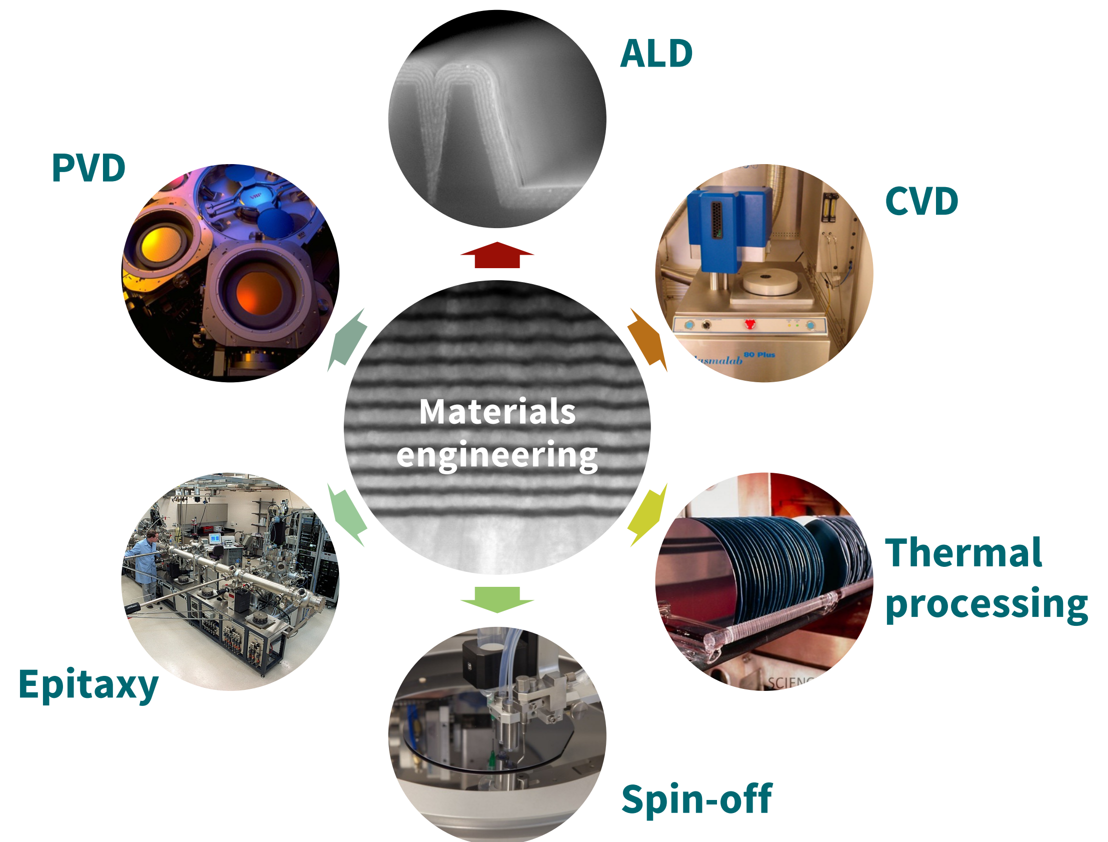

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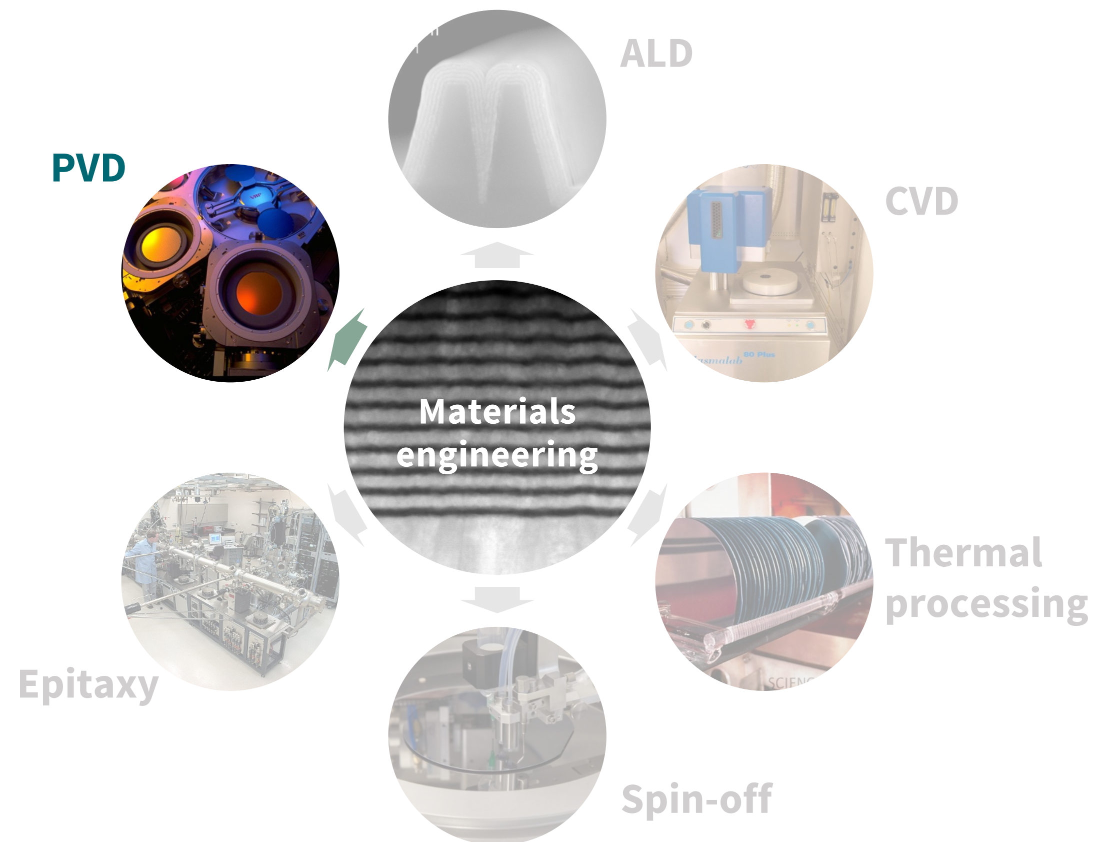
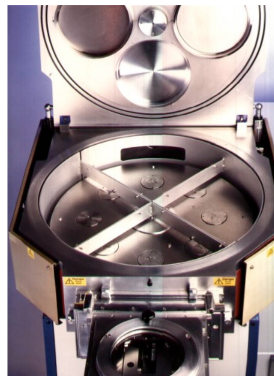


Reactive magnetron sputtering (PVD)

- Versatile technique for the fabrication of semiconductor, dielectric and conductive materials
- Several applications in industry
  - Photovoltaics and anti-reflective coatings
  - Integrated circuits and MOS structures
  - LCD/LED displays
  - Passivation and anti-corrosive coatings
  - Optical and decorative films

photo: Piotr Różański (TRUMPF)



P. Alvarez et al., Oxford Instruments Workshop (2017)

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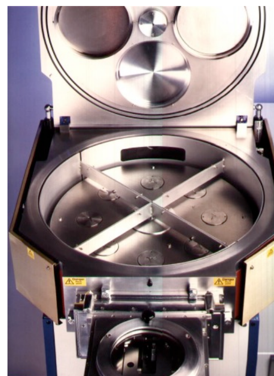

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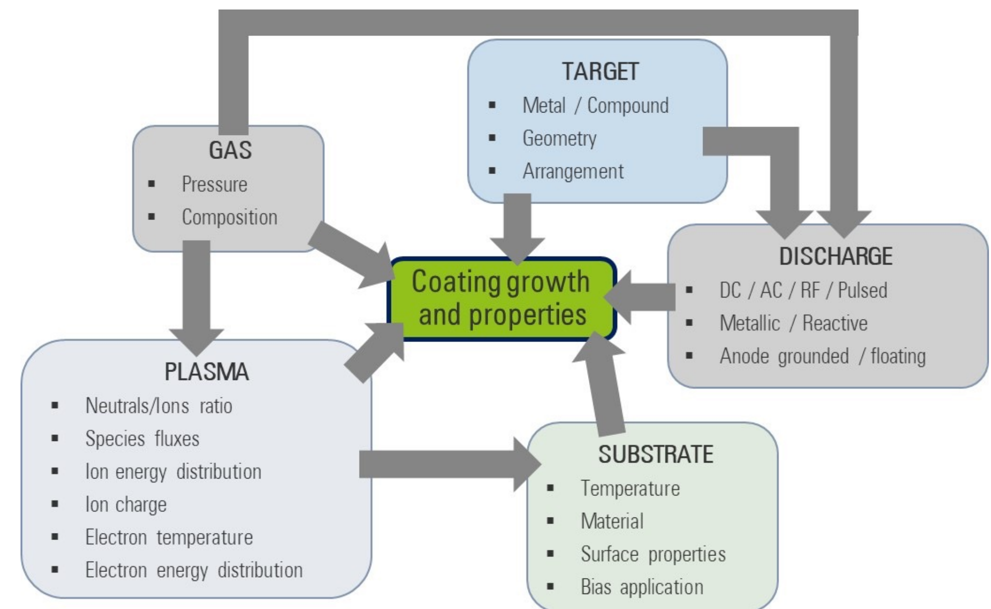
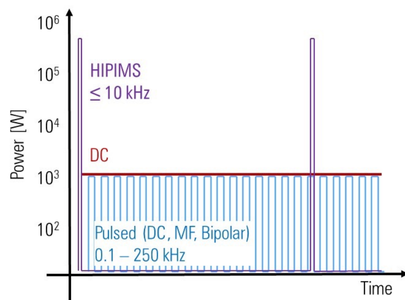


on the basis S. Kadlec et al. Surf. and Coat. Techn., 54/55 (1992) 287-296

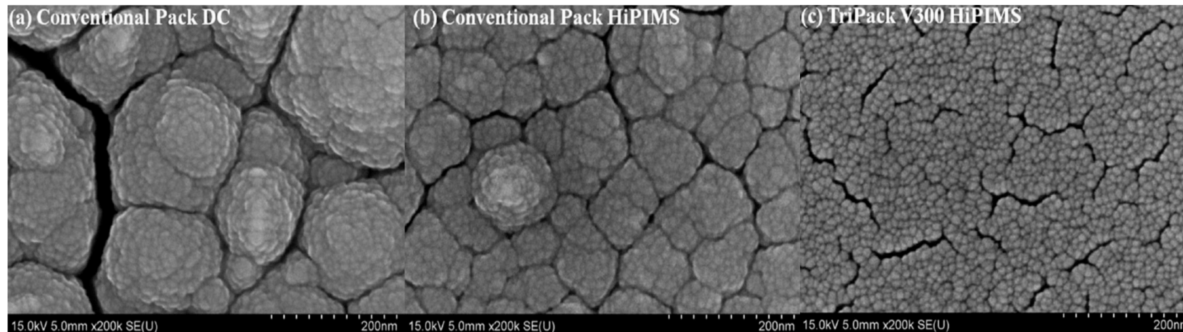
Motivation

- Typically, pulsed magnetron sputtering process used
- Why not to use high-power impulse magnetron sputtering (HiPIMS)?



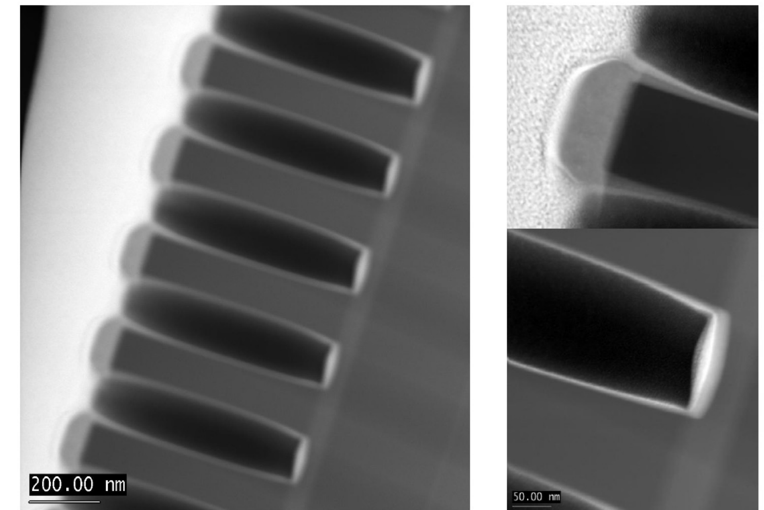
W. Gajewski, R. Mroczyński, M. Puźniak et al., HIPIMS Days Braunschweig, Germany (2019)

TruPlasma 4002 G2, TRUMPF Huettinger



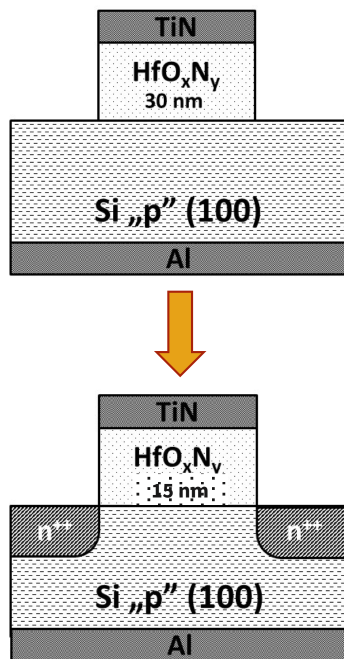
P. Raman et al., J. Appl. Phys. 120, 163301 (2016)

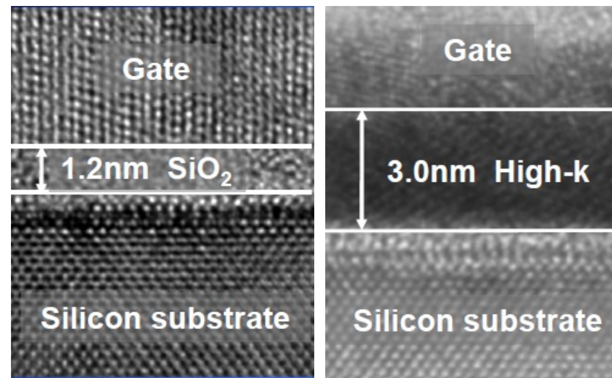
A. Ehiasarian, „Fundamentals of HiPIMS” (2020)



Motivation

- **Aim of this study**: Optimization of ultra-thin hafnium oxynitride films (HfO_xN_y) for a gate dielectric in MOS applications





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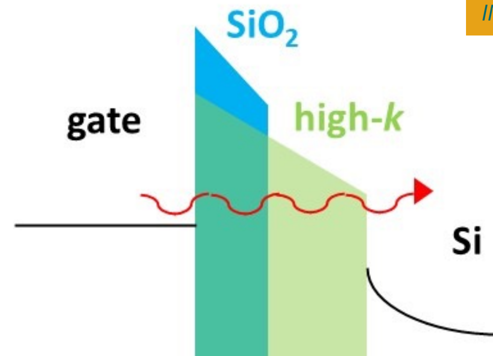
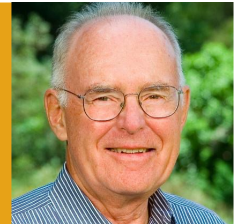
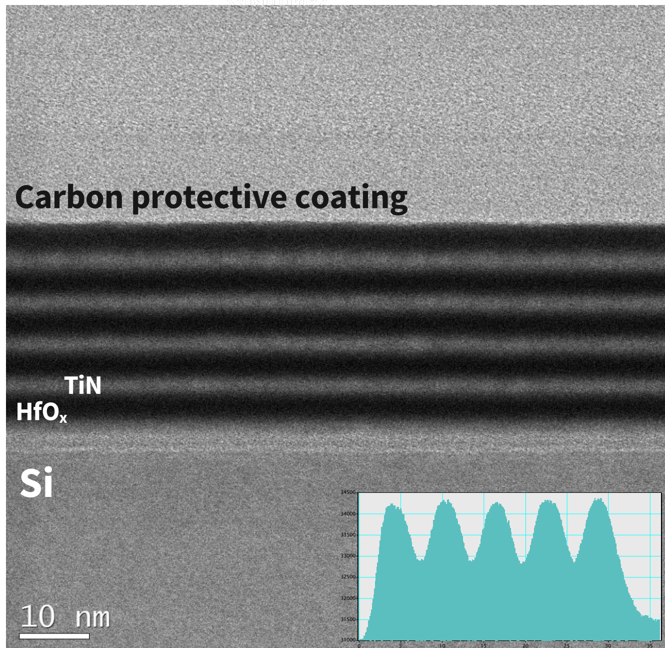


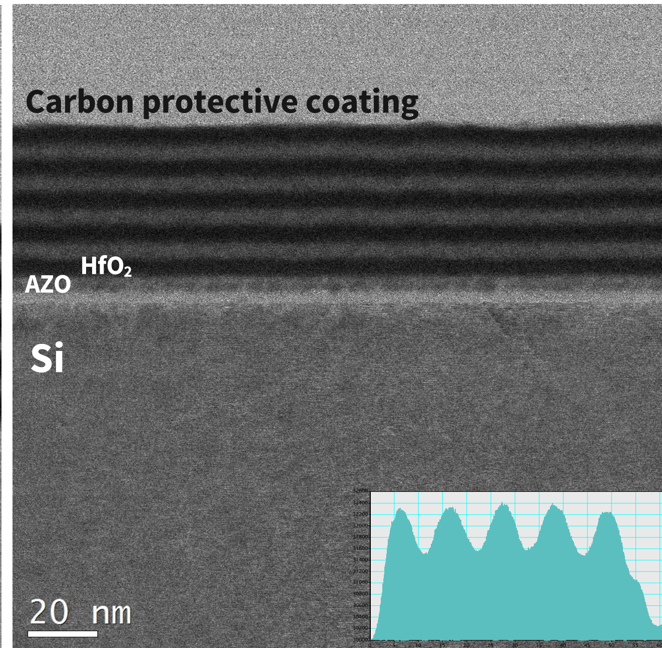
„Hafnium-based high-k + metal gate transistors are the biggest advancement in transistor technology since the late 1960s."
Gordon Moore, INTEL (2007)

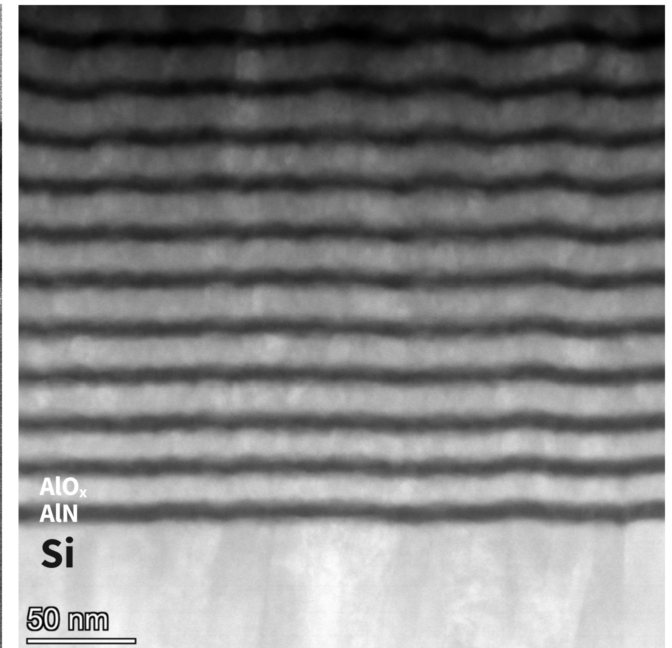


„SiO_2 is at the very heart of the transistor, and replacing it is like performing a heart transplant."
Robin Degraeve, IMEC (2003)

Quiz



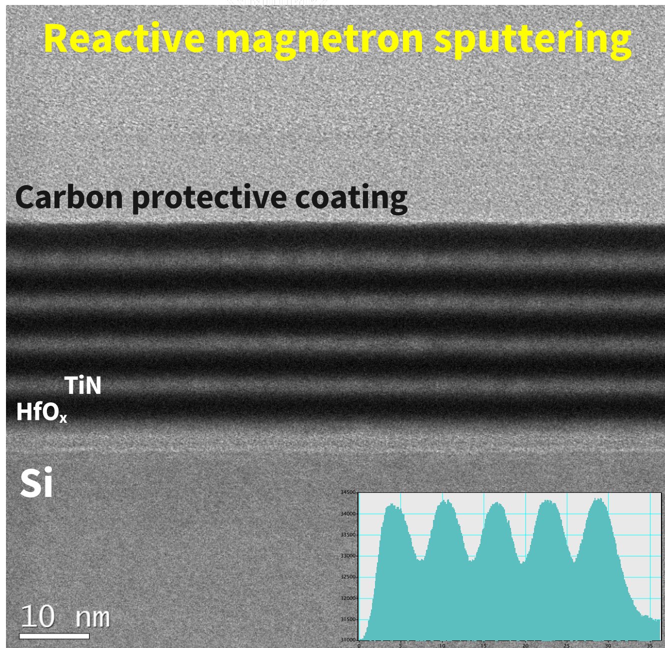


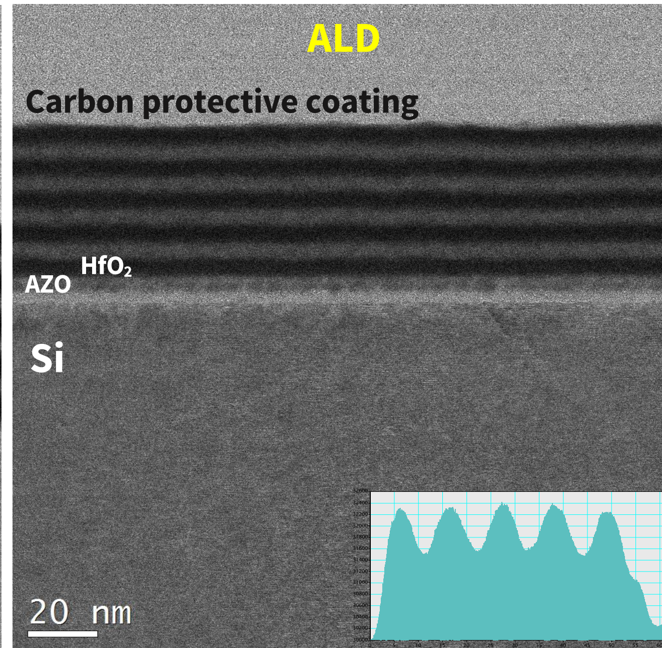


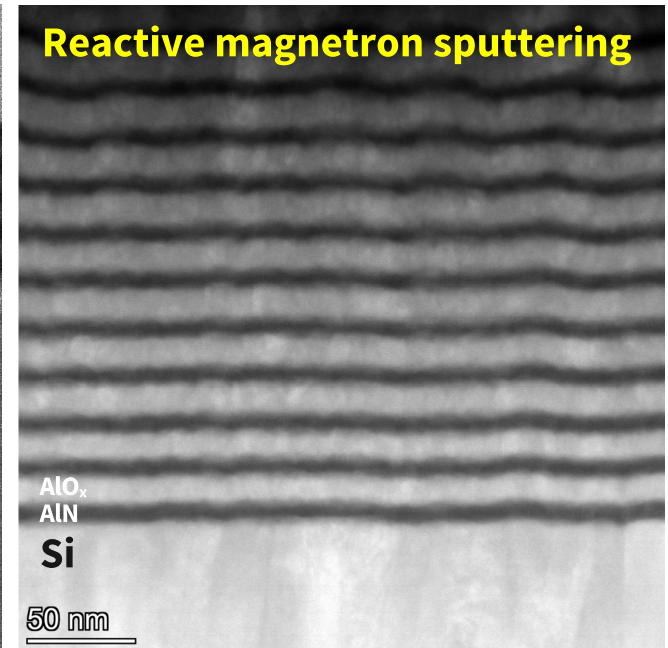
R. Mroczyński, D. Iwanicki, B. Fetlinski, M. Ozga, M. Swiniarski, A. Gertych, M. Zdrojek, M. Godlewski, Crystals 10 (2020) 384

HRTEM photos: M. Andrzejczuk, T. Płociński

Quiz







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HRTEM photos: M. Andrzejczuk, T. Płociński

Taguchi orthogonal tables approach

- The classical approach in process optimization assumes carrying out processing steps taking into account all values of selected process' parameters
- Let's assume we optimize 4 input (process) parameters each with 3 variables

number of parameters

$$3^4 = 81$$

experimental runs

number of variables

- In this case we need to perform 81 experimental runs

		A1			A2			A3		
		B1	B2	B3	B1	B2	B3	B1	B2	B3
C1	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X
C2	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X
C3	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X

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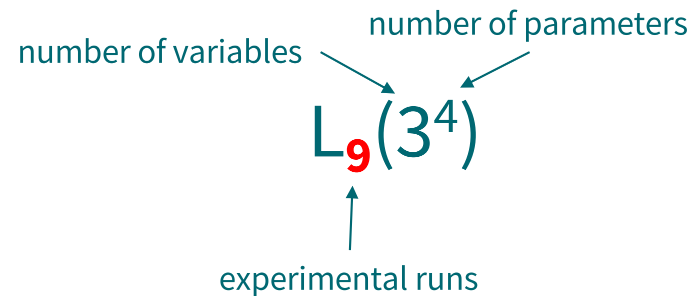
number of variables

- In this case we need to perform 81 experimental runs
- **It's safe**
- **Expensive**
- **Time-consuming**

		A1			A2			A3		
		B1	B2	B3	B1	B2	B3	B1	B2	B3
C1	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X
C2	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X
C3	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X

Taguchi orthogonal tables approach

- Taguchi orthogonal tables approach utilize the mathematical prove that not every experimental run is equally important, and some could be skip
- The errors due to the omitting some experimental runs reduce each other



- Significant reduction of experimental runs!

		A1			A2			A3		
		B1	B2	B3	B1	B2	B3	B1	B2	B3
C1	D1	**X**	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	**X**	X	X	X
	D3	X	X	X	X	X	X	X	**X**	X
C2	D1	X	X	X	X	X	X	X	X	**X**
	D2	X	**X**	X	X	X	X	X	X	X
	D3	X	X	X	**X**	X	X	X	X	X
C3	D1	X	X	X	X	**X**	X	X	X	X
	D2	X	X	X	X	X	X	**X**	X	X
	D3	X	X	**X**	X	X	X	X	X	X

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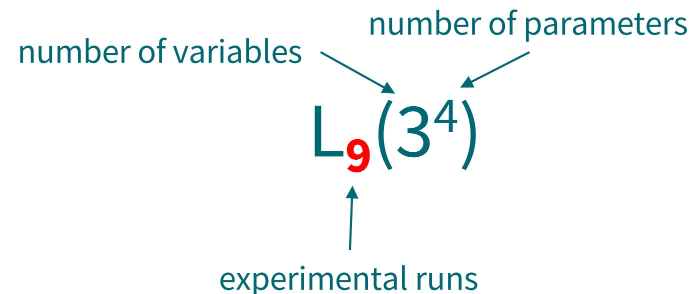

- Significant reduction of experimental runs!
- **Orthogonal tables!**

	Pressure (mTorr)	HiPIMS Power (W)	Oxygen (O_2) flow (sccm)	Nitrogen (N_2) flow (sccm)
Var 1	3	300	5	5
Var 2	6	500	10	10
Var 3	9	700	15	15
Run 1	3	300	5	5
Run 2	3	500	10	10
Run 3	3	700	15	15
Run 4	6	300	10	15
Run 5	6	500	15	5
Run 6	6	700	5	10
Run 7	9	300	15	10
Run 8	9	500	5	15
Run 9	9	700	10	5

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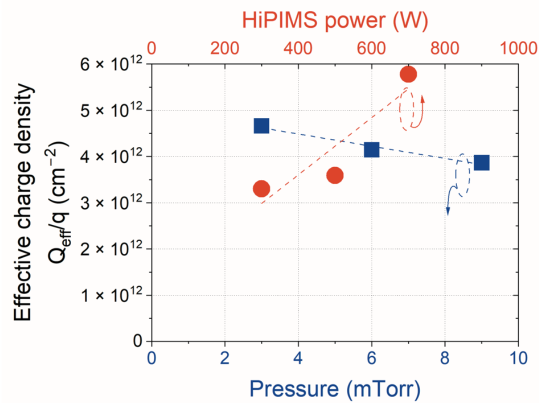

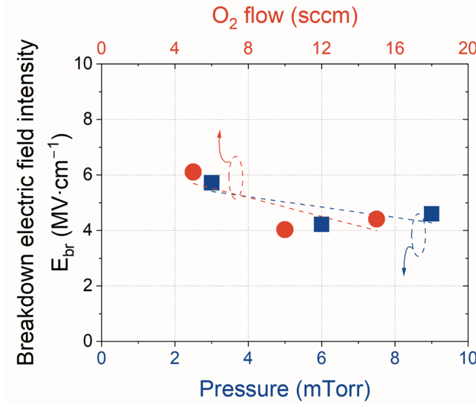

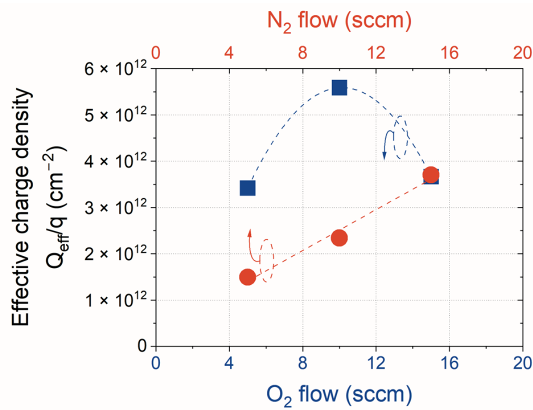

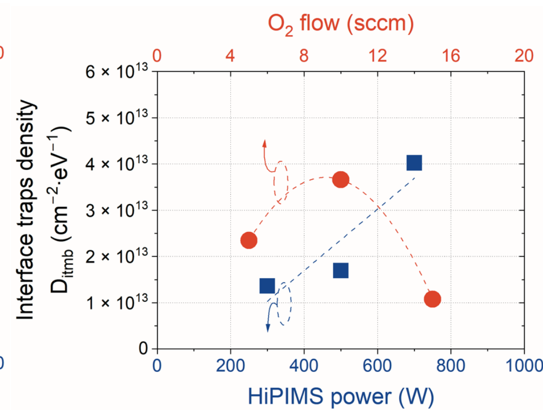

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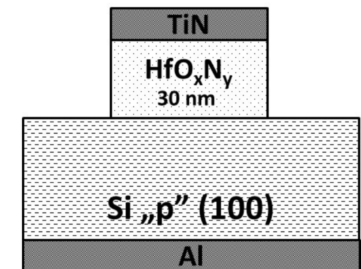
Electrical characterization of fabricated devices

- MOS structures fabricated
- 30 nm HiPIMS HfO_xN_y films used as gate dielectric layer
- C-V / I-V measurements analysis
- Thermal stability up to 800ºC investigated
- The two sets of HiPIMS processes were designed to obtain dielectric materials with (1) good electrical parameters (i.e., **optimal process**), and (2) intentionally deteriorated electrical parameters (i.e., **non-optimal process**)



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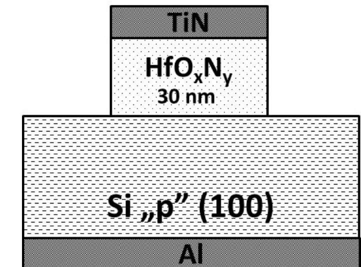

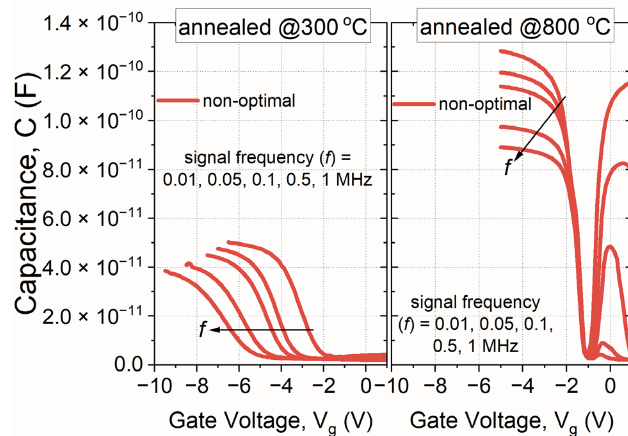

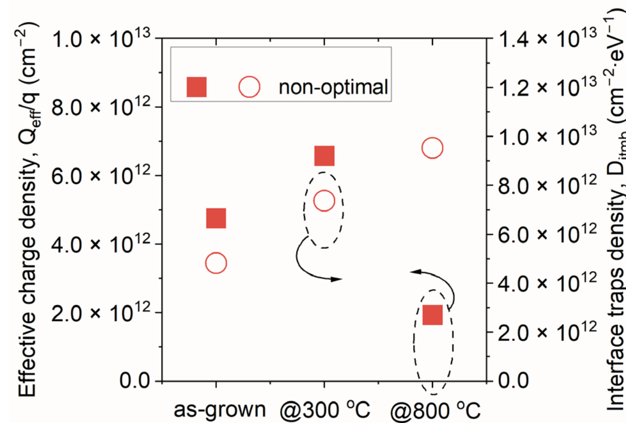

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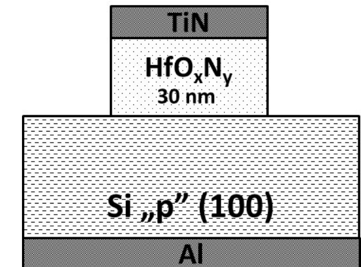

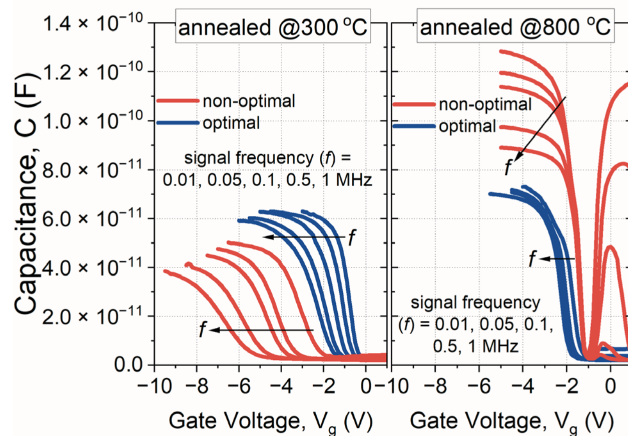

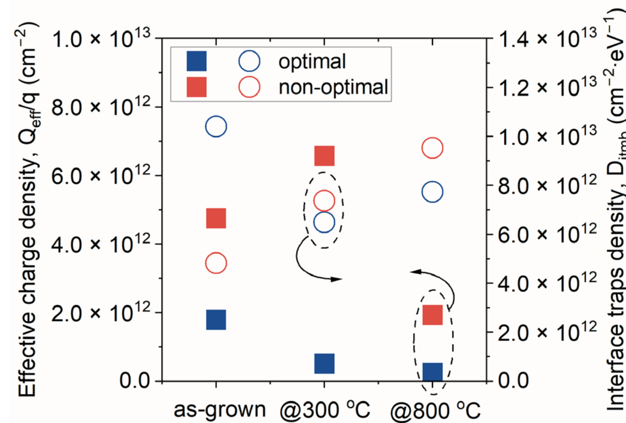

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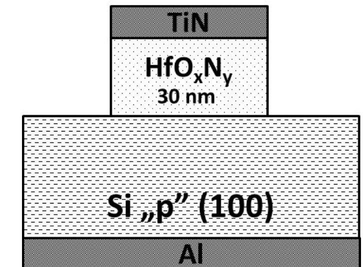

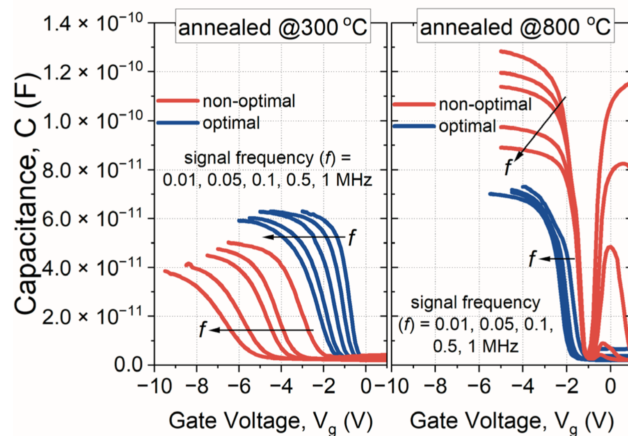

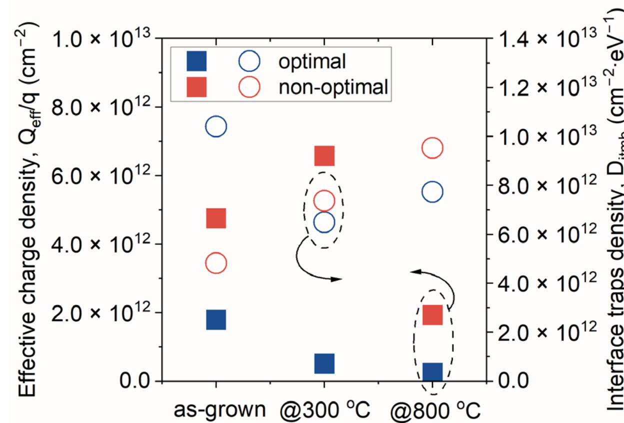

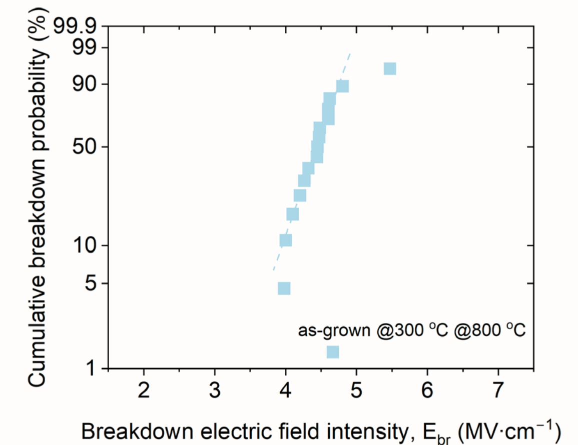

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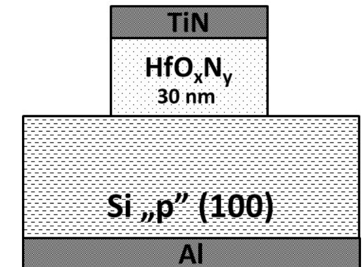

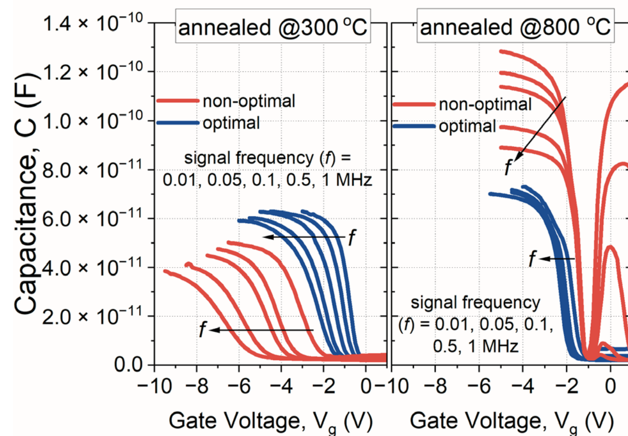

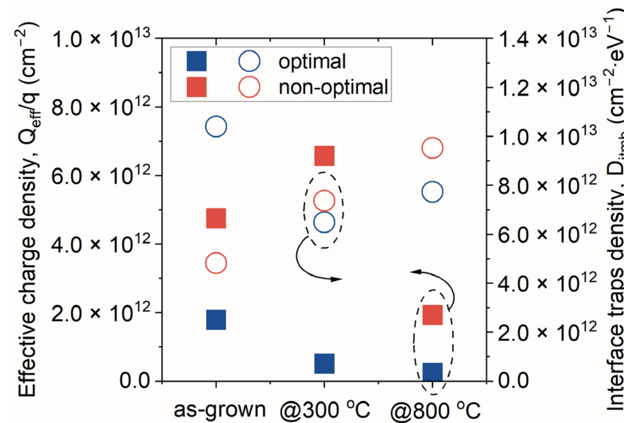

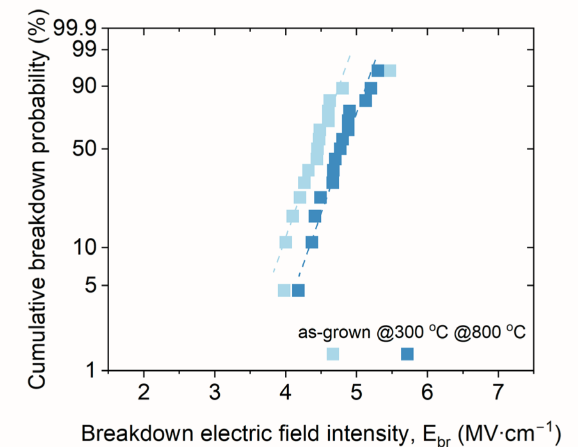

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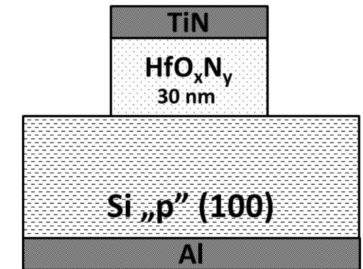

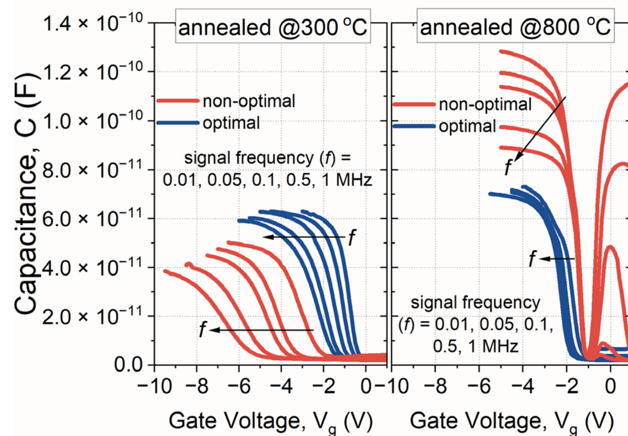

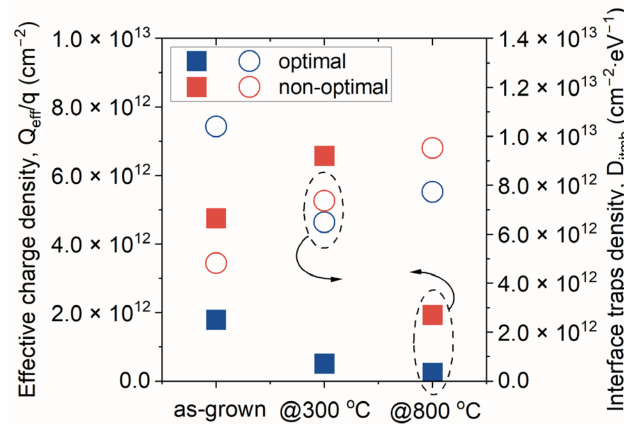

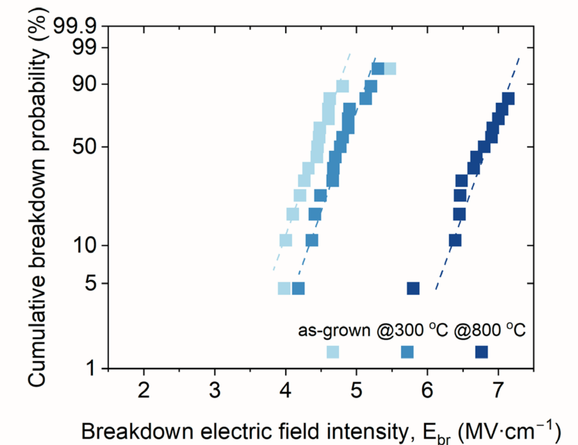

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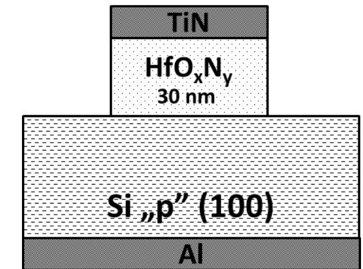
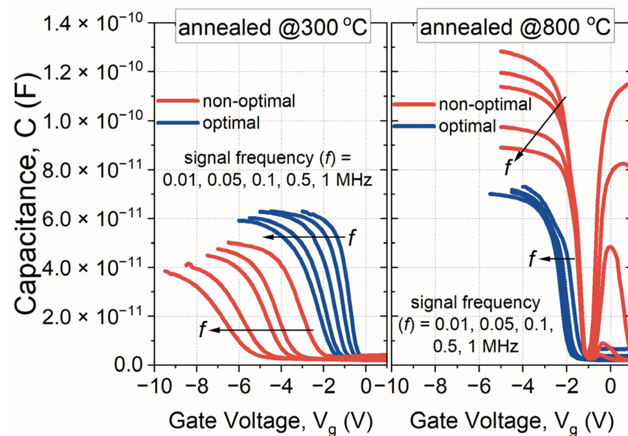
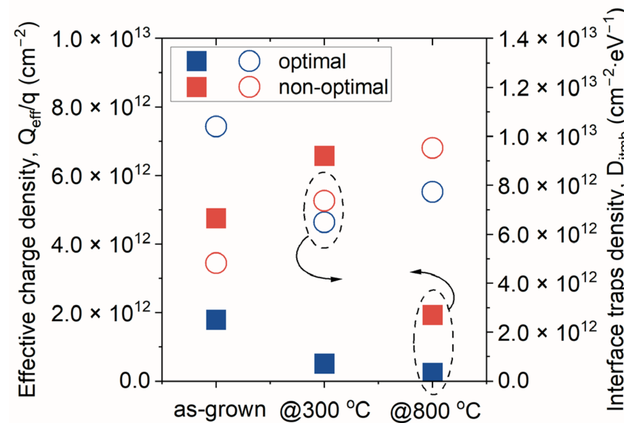
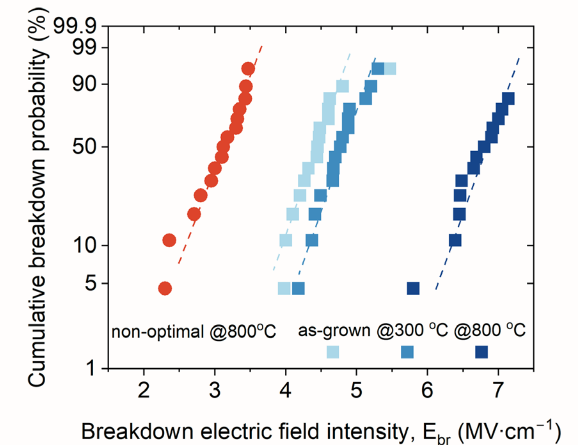


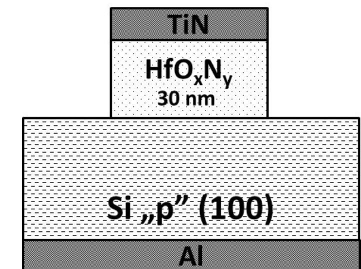


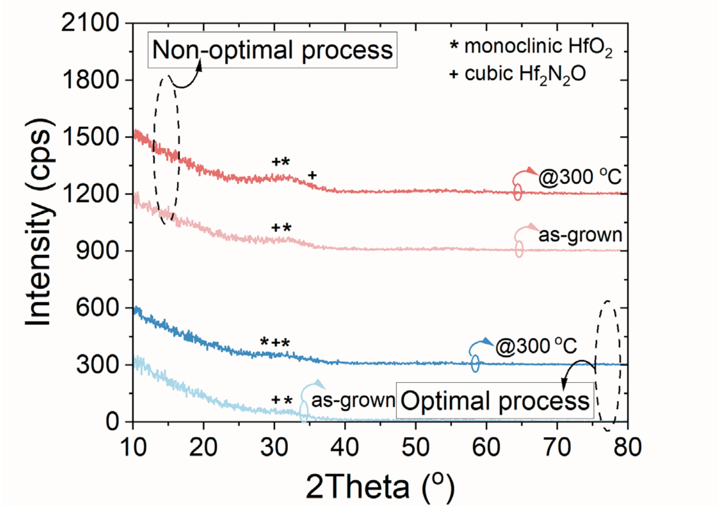




Structural characterization of obtained materials

- Grazing-angle incidence X-ray diffraction (GIXRD), X-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM) allowed the identification of changes in structure and chemical composition of investigated materials





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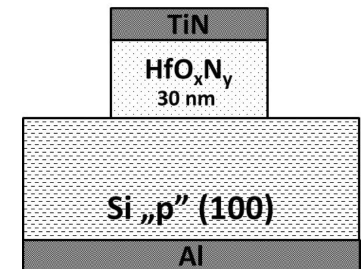

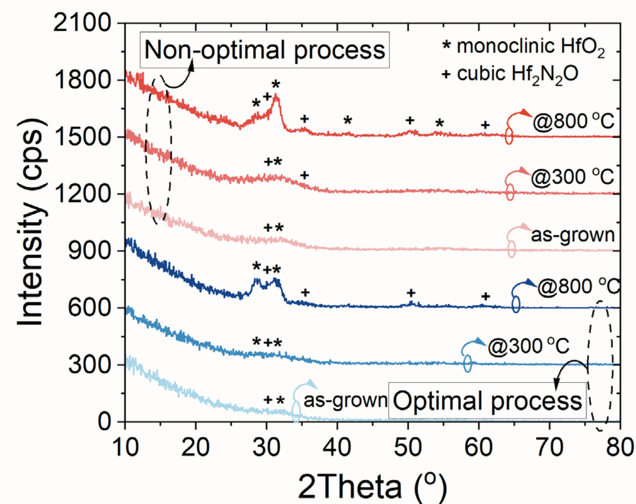

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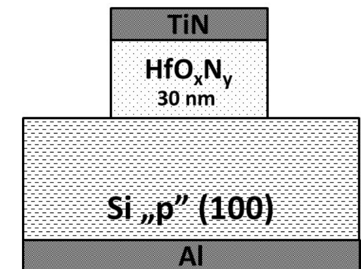

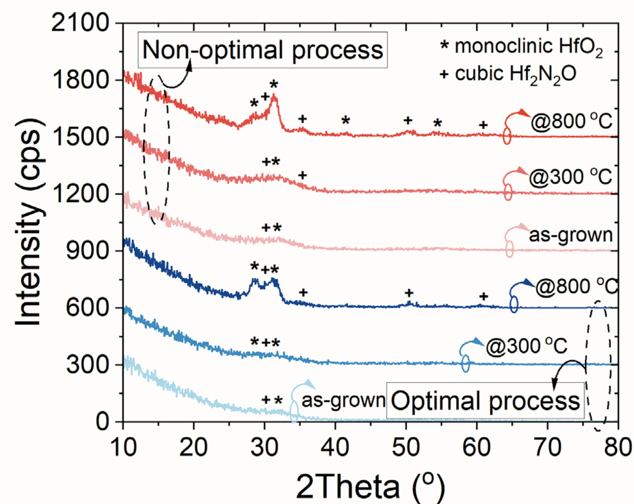

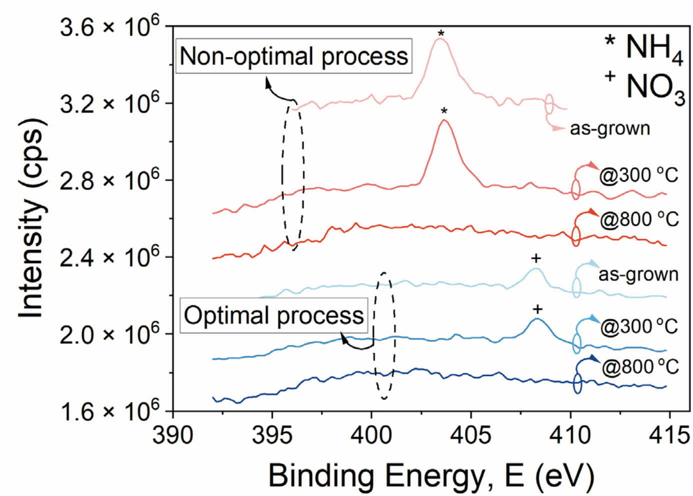

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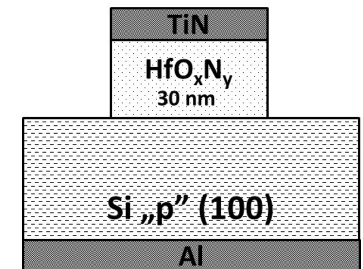

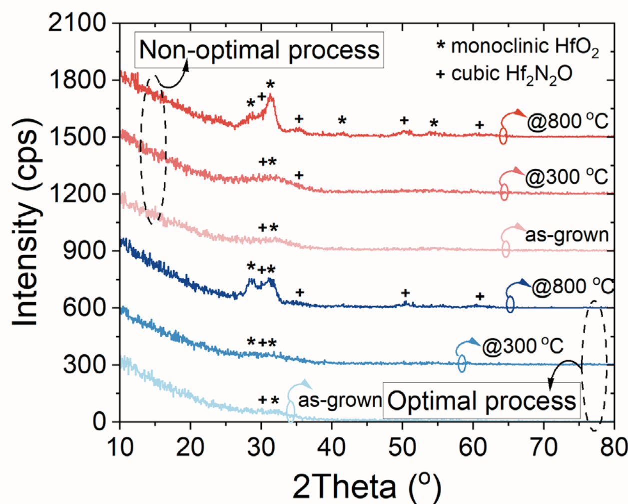

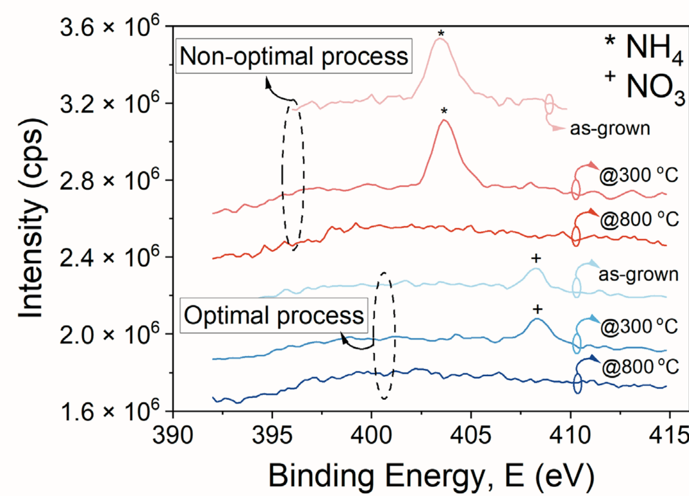

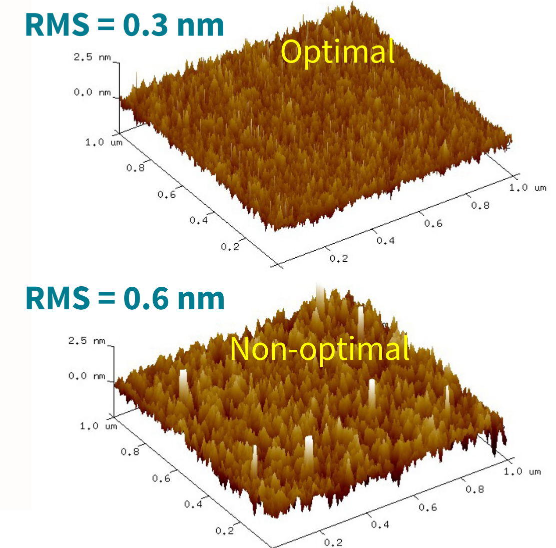

MOSFETs fabrication and characterization

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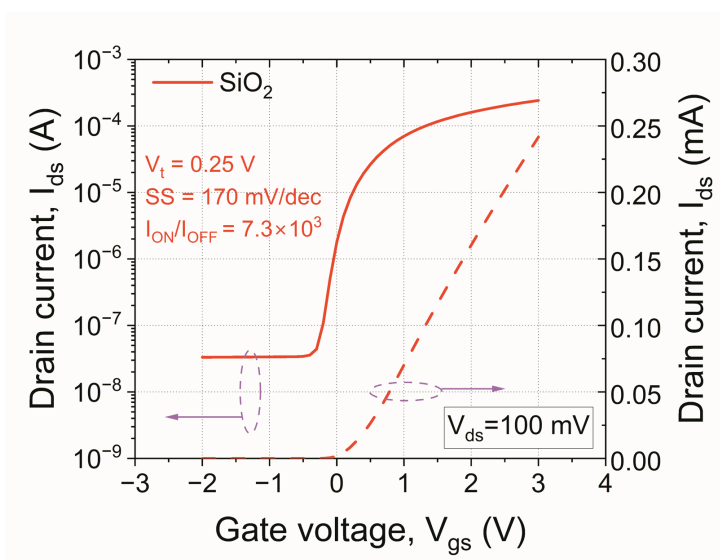

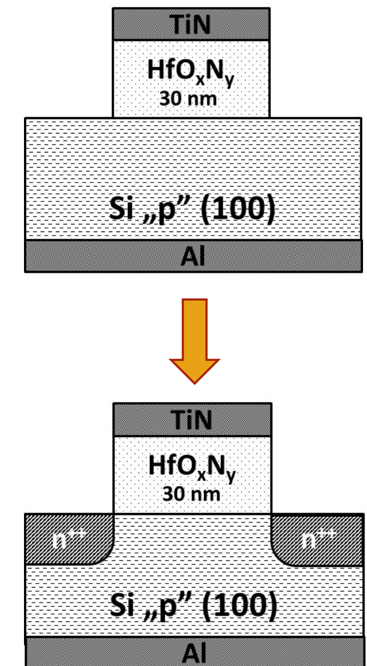

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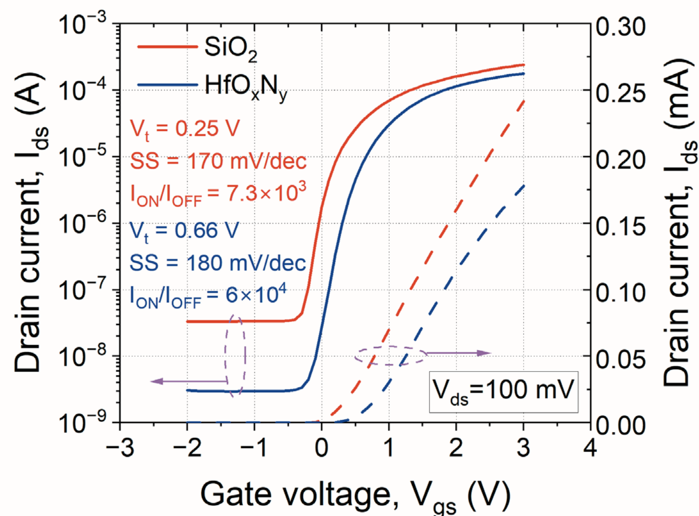

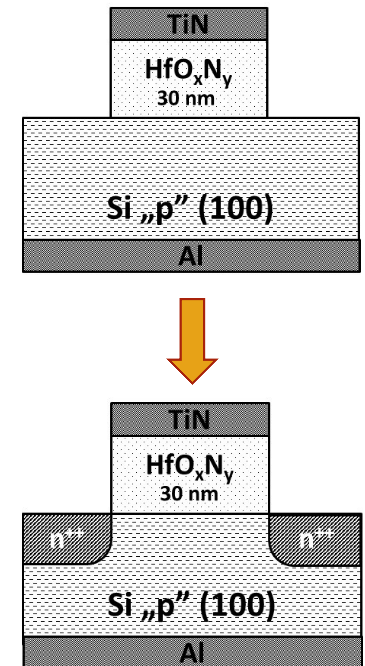

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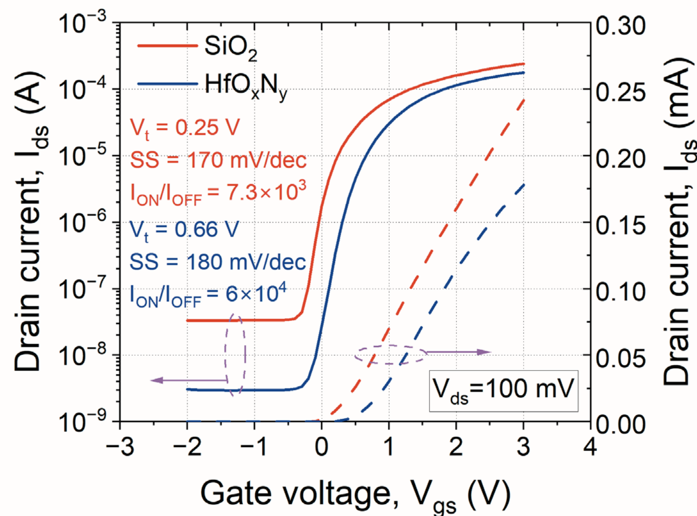

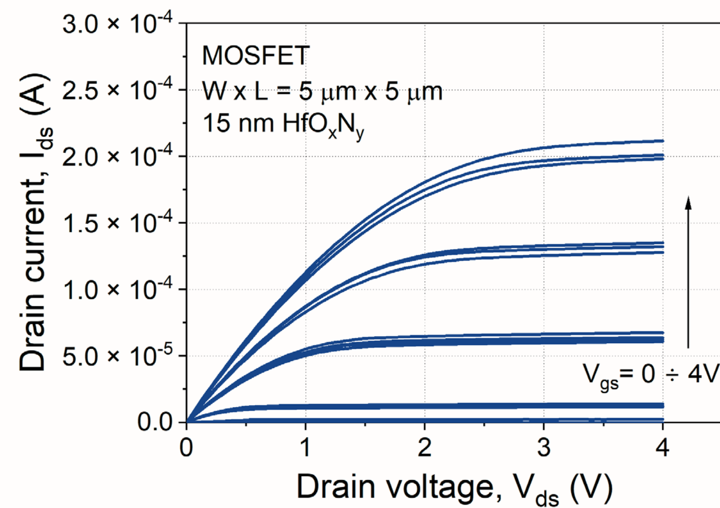

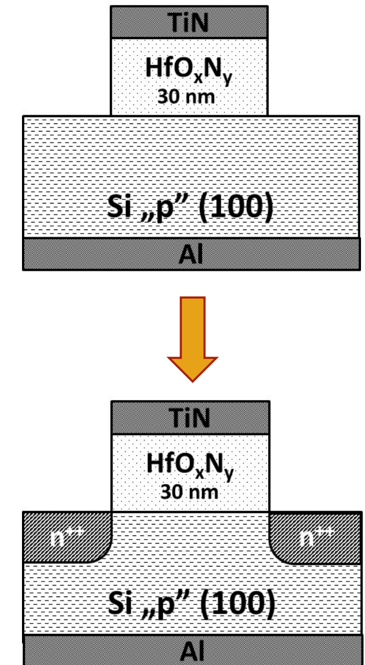

Conclusion

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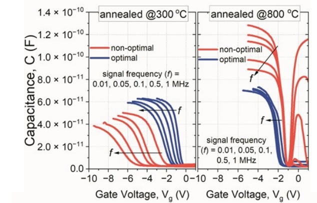
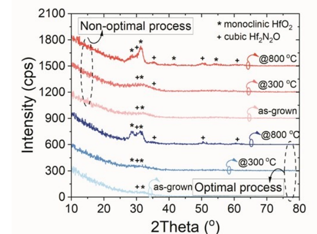
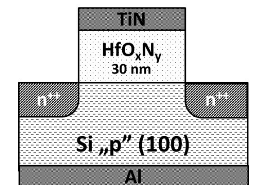
  - Successful optimization of HiPIMS process by employing Taguchi orthogonal tables approach
  - Analysis of thermal stability of deposited thin films
  - Identification of structural changes due to the thermal treatment and correlation with electrical parameters of MOS structures
  - Compatibility of developed HiPIMS HfO_xN_y processing with self-aligned FET devices technology

		A1			A2			A3		
		B1	B2	B3	B1	B2	B3	B1	B2	B3
C1	D1	**X**	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	**X**	X	X	X
	D3	X	X	X	X	X	X	X	**X**	X
C2	D1	X	X	X	X	X	X	X	X	**X**
	D2	X	**X**	X	X	X	X	X	X	X
	D3	X	X	X	**X**	X	X	X	X	X
C3	D1	X	X	X	X	**X**	X	X	X	X
	D2	X	X	X	X	X	X	**X**	X	X
	D3	X	X	**X**	X	X	X	X	X	X







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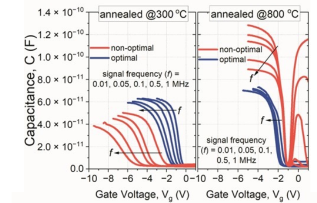
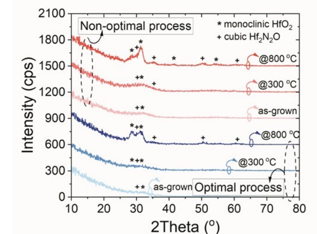
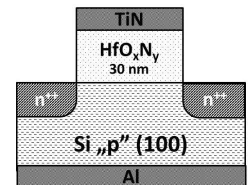
- **Key message**
    - **There is a plenty of room for HiPIMS processing in novel semiconductor devices technologies !**

		A1			A2			A3		
		B1	B2	B3	B1	B2	B3	B1	B2	B3
C1	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X
C2	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X
C3	D1	X	X	X	X	X	X	X	X	X
	D2	X	X	X	X	X	X	X	X	X
	D3	X	X	X	X	X	X	X	X	X







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