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Upscaling Challenges of HIPIMS for Directional Deposition

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ABSTRACT

Ionized deposition based on HIPIMS has been successfully developed for barrier and copper seed layers in Through Silicon Vias with very high aspect ratios of 10:1 and up to 20:1. However, upscaling to larger substrate sizes like 300 mm wafers generated several process challenges. In HIPIMS with static deposition mode the required pulse peak currents get quite high due to large target areas. The substrate bias had to ensure that a high fraction of the ionized metal is directed towards the substrate and not towards the target, because for materials with high sputter yield the ionization degree is reduced by self-sputtering. For uniformity optimization the contributions of metal ions and metal atoms had to be treated separately to achieve uniform seed layers in the vias and in the field of the substrate. The new process was applied to 200 x 10 µm vias on 300 mm wafers and the seed layers were enforced by Cu electroplating. The results were analyzed by cross-section SEM prior to and after electroplating. X-ray tomography was applied for nondestructive inspection of the entire wafer and to demonstrate that all vias had been properly seeded in the entire depth of the via.

INTRODUCTION

One of the major and most attractive features of HIPIMS is its capability of directional deposition in vertical structures with very high aspect ratios. As miniaturization of microelectronics is approaching the physical limits and lateral wiring gets more and more challenging, vertical interconnects in microelectronic chip stacks have been developed known as 3D-integration using Through Silicon Vias (TSV) as described in [1,2]. This technology has the advantage of improving the electrical performance and enabling heterogeneous integration. Directional deposition methods have already been developed for CMOS manufacturing, but the needs for emerging 3D- integration are quite different. In TSVs high aspect ratios in the range of 5 to 10 or even higher are being requested together with via diameters in the range of 10µm. 3D- integration is also extremely cost-sensitive compared to front- end CMOS manufacturing so that appropriate PVD equipment and processes should be developed accordingly.

Leveraging the inherent advantages of HIPIMS, a modified technology has been developed at Evatec for 3D-integration on silicon wafers (up to 300 mm in diameter) which is known as HIS (Highly Ionized Sputtering) [3]. While in other applications, like hard coatings, the upscaling of the HIPIMS process can take advantage of a moving or rotating substrate, 3D-integration of Si wafers requires stationary deposition and the Evatec HIS solution therefore uses single wafer chambers to minimize particle generation. This technique minimizes contamination of the high value wafers, which could be at risk in a batch type coating tool.

Due to the much closer target-to-substrate distance compared to more traditional directional techniques, the specific deposition rates, target utilization rates and target lives of HIS are high and other consumable costs, like the volume of shields to be cleaned, power and coolant consumption are low. As the power supply is switchable to DC the process module can also be easily used as a standard PVD chamber, e.g. for redistribution layers (RDL), without even the need for chamber venting. The investment required to maintain a 3D integration line is therefore minimized since the same tool can be used for several directional and non-directional PVD processes.

EXPERIMENTAL METHODS

Substrates

Silicon wafers with 300 mm diameter and dense TSV test patterns having via diameters of 10 µm and aspect ratios up to 20:1 were used for process qualification.

Seed Layer Deposition

Metal adhesion layer of titanium, or alternatively tantalum as barrier layers, and copper seed layers for electroplating were deposited in an Evatec CLUSTERLINE®300 tool configured with standard PVD chambers upgraded to the HIS configuration including the appropriate RF bias application. For substrate cooling the PVD stations were equipped with electrostatic chucks (ESC), which are vitally important

especially for thicker Cu layers. The complete integrated process sequence consisted of the following steps: Degas - ICP Etch Clean - HIS Ti (or Ta) - HIS Cu. Copper is the preferred metal for through-wafer interconnects due to its low resistivity and low electromigration characteristics. It is widely used in wafer packaging and also in on-chip interconnects. In the CLUSTERLINE®300 target diameters of 400mm are used, which is comparatively small for 300mm substrates and therefore provides a cost-effective solution. However to reach the HIPIMS mode on this target area a peak current close to 1000 A has to be used.

Process Integration

TSV fabrication and filling was done on fully automated semiconductor processing equipment. The vias were etched using a Bosch deep reactive ion etch process on an Applied Materials Centura platform. Oxide liners were deposited by sub-atmospheric chemical vapor deposition (SACVD) using tetraethylorthosilicate (TEOS) and ozone on an Altatech tool. The SACVD produces smoother films than PECVD, which is especially required on the sidewalls, where the Bosch process usually leaves some scallops. Electroplating was carried out in an Applied Materials Raider-S platform with "Superfill" capability.

Sample Characterization

PVD samples were cleaved and analyzed for sidewall and bottom coverage in a Zeiss Leo 1560 SEM. Copper filled TSVs were cleaved, ground, polished and analyzed by optical microscope. In addition to this a Nordson Dage Diamond X-ray CT tool was used for the non-destructive verification of void-free plating.

OPTIMIZATION OF THE *HIS* PROCESS

The Uniformity Issue

As reported in previous publications [3] it is generally observed for circular sputter sources that when moving from standard PVD to HIPIMS the deposition profile is increasingly dome shaped with higher peak currents. One possible explanation for this effect is that the magnetic field is attenuated by the opposed magnetic field which is generated by the high drift current of the magnetron. It has been shown that the drift current of the HIPIMS discharge is a factor of 2 higher than the current to the cathode [4], so that the drift current will be well above 1000 Amps.

The usual method to compensate from a dome shaped to a flat uniformity is the design of the rotating magnet, which typically has a kidney shape. While this works pretty well for Ti and Ta, it is more difficult for Cu due to the self-sputter yield of Cu being more than 4 times higher compared with Ti [5]. This means that the metal ions which are generated by the HIPIMS discharge are partly accelerated towards the target and generate there – in the case of Cu – a relatively high ratio of neutral Cu atoms, described in [5] as "return effect", thus lowering the total ionization degree. Consequently even though Cu is easier to ionize, the ionization degree is significantly lower in a HIPIMS discharge compared to Ti. As a result of these material properties, for high aspect ratio vias such as 10:1 the step coverage for Ti and Ta is typically a factor of 2 better than for Cu in the HIPIMS process. As a consequence, when a rotating magnet is optimized to provide a uniform metal layer a deficiency of metal ions may occur in the target center. As shown in the left part of Figure 1 the lower ionization degree then results in an insufficient Cu seed layer in the wafer center (as indicated by the yellow circle in Figure 1), so that the electroplating process is not able to reach the bottom of the via there. However, with the appropriate magnet design together with an operative RF application a uniform ion current can be achieved over the entire 300 mm substrate, so that an effective electroplating process is guaranteed, while still having good uniformity of less than ±5% in the field.

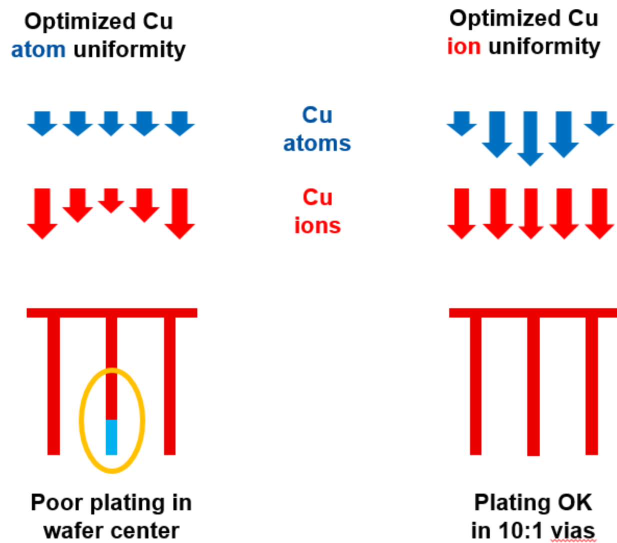

Figure 1. The effects of radial neutral and ion distributions on the seed layer quality of a larger substrate

The Target Life Issue

The erosion of the target during production results in grooves on the sputtered target surface, which cannot be neglected since target thicknesses of up to 25 mm may be used. In order to compensate for the edge effect on uniformity, the erosion pattern typically consists of an outer main erosion groove and

at least one weaker inner erosion groove towards the center of the target. The outer main erosion groove is required for a good deposition uniformity to cope with the limited target diameter. Since throughout target life this main erosion groove will get deeper more quickly, the magnetic field becomes significantly stronger in this location. As a result the discharge current rises and the voltage decreases for a fixed discharge power. Usually the control system of a sputter deposition system runs a user-defined program or recipe and allows adjustment of either deposition time or discharge power to get the same film thickness throughout the entire target life. In many applications a change of the voltage/current ratio is no problem since the rate is defined by the discharge power. The ratio of inner to outer magnet strength can however affect the uniformity over target life. A device for adjusting the magnet distance to the target effective on parts of the magnet assembly, like described in [6], can be applied to correct the uniformity. Such a magnet lift device is especially required for HIPIMS processes, since the current rise – and therefore the peak current - is strongly dependent on the applied voltage, as plotted in Figure 2 for 100 µsec pulses. Now if the target voltage changes due to target erosion and the resulting magnetic field and impedance change, it gets impossible to enable a constant HIPIMS process over the entire target life. The peak current is directly correlated with the ionization degree of the discharge and the ionization degree itself and is the driving parameter to enable the seed layers in high aspect ratio vias.

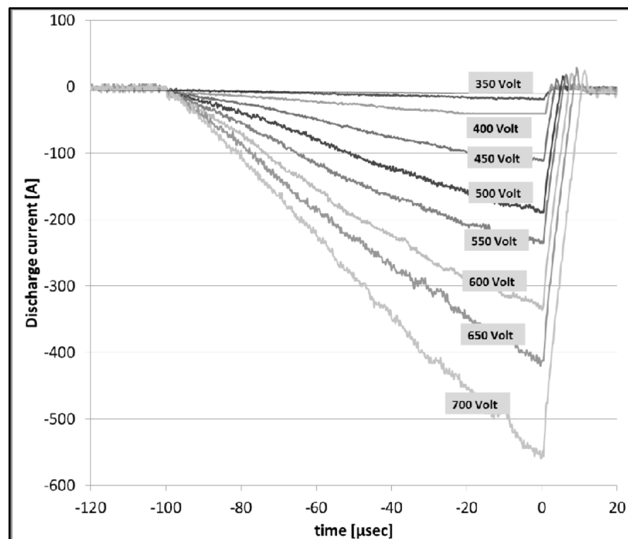

Figure 2. The current rise as a function of the applied target voltage 100 µsec pulse.

Figure 3 shows schematically the evolution of 100 µsec pulse shapes over the target life, where not only the peak current will increase but also the pulse shape will change as soon as the operation limit or the arc level of the power supply is approached.

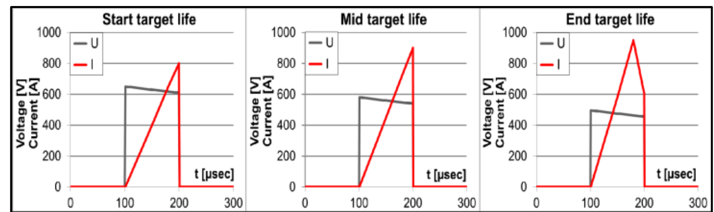

Figure 3. Schematic evolution of voltage and current for a HIPIMS process with a 100 µsec pulse over target life without magnet change running with a constant pulse power and the peak current reaching the operating limits close to target end.

The solution to this target life effect is a magnet lift, which is active only on the outer portion of the rotating magnet where the main erosion occurs, as sketched in Figure 4. The upper part of Figure 4 shows the new target, where the inner and the outer portion of the rotating magnet are on the same level. In the lower figure, the magnetic field strength is getting stronger, in particular in the main erosion groove. Consequently the outer portion of the rotating magnet is retracted to reduce the magnetic field strength. In Figure 5 a uniform pulse shape achieved by a magnet readjustment is plotted schematically, thus providing a stable ionization degree and uniformity over the entire target life.

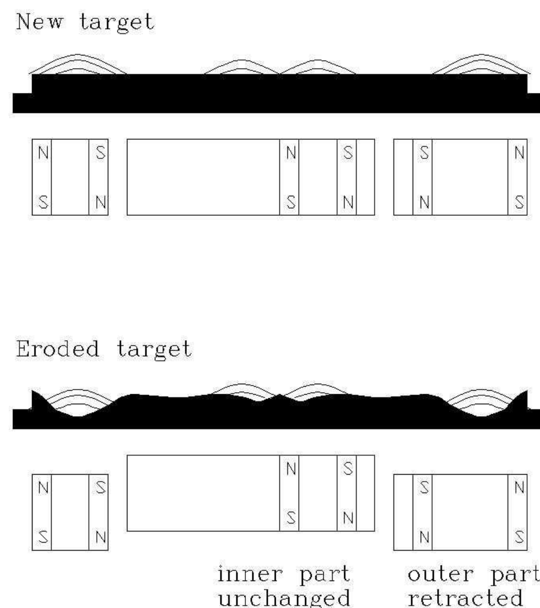

Figure 4. The principle of the outer magnet lift.

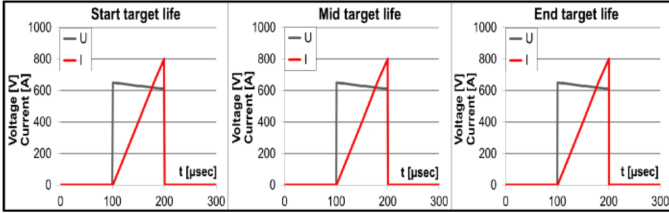

Figure 5. Schematic evolution of voltage and current pulse shapes achieved by a magnet life readjusted over target life.

RESULTS

Overview of the Developed Processes

Table 1 summarizes the process characteristics of the qualified processes. The deposition rates for the HIS process in TSV applications is approx. 50% of that of the qualified DC process, which is used for RDL applications. HIS deposition rates are typically 3 nm/s for Ti and 10 nm/s for Cu. However due to temperature limitations, cooling step interrupts may also be applied on TSVs if a 2 µm Cu via has to be deposited. Resistivity and stress remain the same for the HIS and DC process (see Table 1). As it can easily be seen, the compressive stress of Ti and the tensile stress of Cu almost compensate for a typical film stack of 0.3µm Ti and 2µm Cu. Table 1 also presents a process for α-Ta, which uses an extremely thin TaN seed layer and has been described in [7]. While standard DC sputtering at low temperatures usually result in β-Ta with a resistivity of up to 200 µΩcm, the α-Ta applied by HIS gives 26 µΩcm. It is assumed that the ionized metal provides the required energy to form α-Ta without any substrate heating. The low resistivity and the expected high density make HIS α-Ta a very attractive candidate for diffusion barriers in Advanced Packaging, where temperatures below 200 or 300°C are requested.

Application on Very High Aspect Ratio Vias

The optimized process was applied to a film stack of 0.3 µm Ti and 2.2 µm Cu on test wafers with a via opening diameter of 10µm and via depths ranging from 120 µm to 200 µm. The bottom and the sidewall coverage relative to the film thickness in the field of the wafer were measured by SEM cross sections and are plotted in Figure 6. As it can be seen the sidewall coverage is at 1% between aspect ratios from 5:1 to 20:1, while the bottom coverage decreases with increasing aspect ratio. These results show that the ionized material enters the via with a very high directionality and that it remains “trapped” in the lower portion of the via. With 2.2 µm Cu in the field the sidewall coverage is more than 20 nm in all locations. It was found that “Superfill” electroplating requires a minimum of 20nm to provide a flawless film. Figure 7 shows a via with aspect ratio 20:1 electroplated with a few µm of Cu, showing that the chemistry employed in the plating bath is already reaching its limits keeping the via mouth open.

Since one cross section of one selected via may not give a picture of the completeness of electroplating over the whole 300 mm wafer, this was subsequently verified by non-destructive X-ray tomography. Figure 8 shows images produced by this method from the wafer center (top) as well as from the wafer edge (bottom), where each “needle” represents a filled via.

Table 1. Characteristics of the qualified processes

Film	Dep. Rate [nm/s]	Resistivity [µΩcm]	Min. step coverage [%]	Stress [MPa]
RDL Ti DC	> 6	< 70	n.a.	< 500 compr.
TSV Ti HIS	> 3	< 70	> 2%	< 500 compr.
TSV HIS α-Ta	> 3	< 26	> 2%	< 700 compr.
RDL Cu DC	> 20	< 2.7	n.a.	< 200 tensile
TSV Cu HIS	> 10	< 2.7	> 1%	< 200 tensile

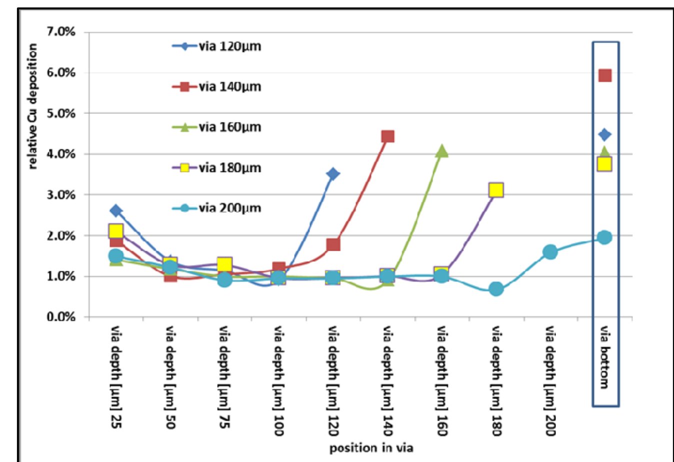

Figure 6. Relative bottom and sidewall coverage in 10 µm vias with depths ranging from 120 µm to 200 µm as measured by SEM cross sections

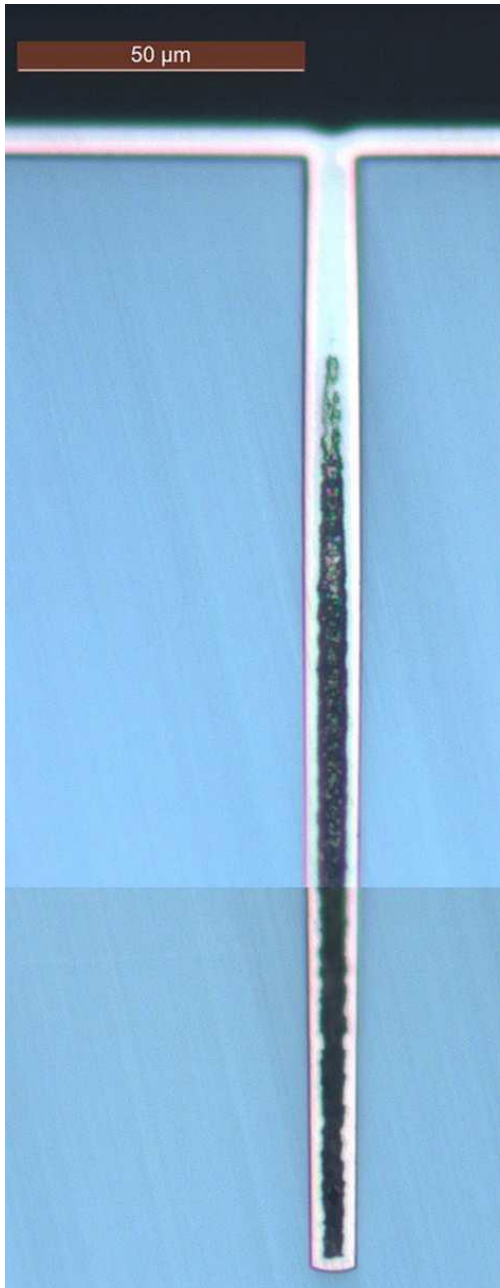

Figure 7. Electroplated via with aspect ratio 20:1 (picture assembled from 2 optical microscope pictures)

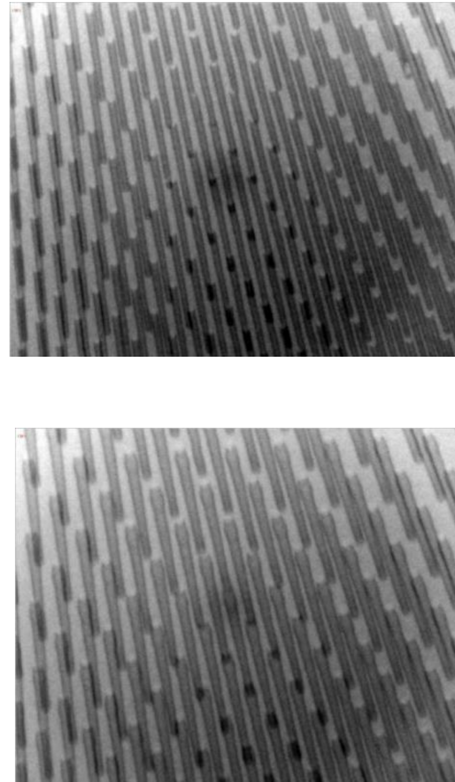

Figure 8. X-ray tomography of liner plated TSVs with aspect ratio 20:1 on the complete 300 mm wafer, top: center of the wafer, bottom: edge of the wafer

CONCLUSIONS

Based on HIPIMS a directional sputtering technology for depositing barrier/seed layers in features with extremely high aspect ratios up to 20:1 has been developed. This so called HIS technology uses basically standard PVD modules, planar targets and a short target to substrate distance. The same module can be used for regular DC sputtering by setting the HIPIMS power supply to DC mode, so that a maximum tool flexibility for additional processes, like RDL, is provided at the lowest cost of ownership. Even for 10x200 µm vias a sufficient seed layer of 20 nm can still be deposited to enable complete electroplating on 300 mm wafers as shown by X-ray tomography. Compared to other directional PVD methods, like Long Throw, Collimator or IPVD, HIS provides the highest directionality of deposition, high specific deposition rates and throughput together with lowest consumable costs, due to a long target life as well as simple and easy to clean shield sets. A novel concept of movable magnets allows deep erosion profiles together with a constant process over target life. HIS provides a superior film texture due to the high ionization, nevertheless the expected improved barrier properties – in particular for α–Ta - still have to be evaluated.

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FOR FURTHER INFORMATION

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