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Millisecond Thermal Processing Using Flash Lamps for the Advancement of Thin Layers and Functional Coatings

Wolfgang Skorupa, Thomas Schumann, Lars Rebohle
Helmholtz-Zentrum Dresden – Rossendorf
Institute of Ion Beam Physics and Materials Research
Dresden, Germany

ABSTRACT

Thermal processing in the millisecond range requires modern, non-equilibrium annealing techniques that allow dedicated material modifications at the surface without affecting the substrate volume below. This process is known as flash lamp annealing (FLA); it is one of the most diverse methods of short time annealing and includes applications ranging from the classical field of semiconductor doping to the treatment of layers on glass, polymers, and other flexible substrates. It extends to other material classes and applications and is of interest to an increasing number of users. Other phrases for FLA used throughout the literature are intense pulsed-light (IPL) sintering and photonic curing.

This paper presents a short and comprehensive view of the current state of the art of FLA with a focus on functional coatings. After an introduction including historical aspects, the paper will cover equipment issues and the pioneering role that semiconductor processing in the framework of advanced chip technology played in the development of short time annealing. Examples of processing for photovoltaics, including doping aspects, hydrogen engineering, copper indium gallium diselenide (CIGS), silicon crystallisation on glass, and transparent conductive oxides (TCO), including indium tin oxide (ITO), zinc oxide (also Al-doped AZO) as well as inkjet printing for flexible electronics, are presented.

INTRODUCTION

The modification of solid material by pulsed light treatments was reported in the 1950s [1]. Short-time annealing–using light sources as a key method of thermal processing of semiconductors was first reported in 1975 by two Russian groups using lasers [2, 3]. The first mention of flash lamp annealing (FLA) in the millisecond range was done by the Novosibirsk group [4].

The transition from the furnace with annealing times of several minutes up to hours and days to the laser with the chance to process materials in the pico- to nanosecond range advanced in the mid-1970s, to the fascination of scientists and engineers who were witnessing a new approach to modifying and manufacturing solid-state materials. Solid-state technology advanced electronics on the micro- and nanoscale. The first review papers on this topic appeared in mid-1980s [5, 6]. During the late 1980s and 1990s rapid thermal processing (RTP) evolved to be the leading technology developed for different aspects of the advanced semiconductor technology. The recent outlook to millisecond processing is reviewed in Refs. [7, 8].

After the development stage, scientific and technological efforts led to a deeper understanding of the effects and mechanisms behind the different versions of short-time annealing. A comparable approach, intense pulsed-light sintering (IPL) for printed or low-cost/large-area electronics was being developed. It was first published by Kim et al. [9]. Another name used for the same approach, photonic curing, was studied by Schroder [10, 11]. A survey of the different short-time annealing approaches is schematically shown in Figure 1. In this figure, RTA is known as rapid thermal annealing.

Short-time annealing processes allow for precise thermal treatment. Millisecond- and nanosecond-scale annealing

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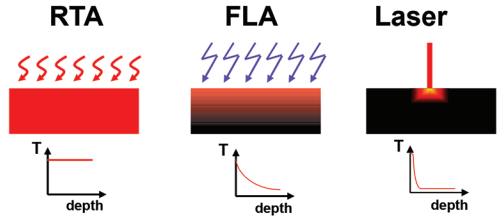

backside	hot	cold	at RT
annealing times	1 – 100 s	100 µs – 100 ms	1 – 1000 ns
light source	halogen lamps	Xe lamps	pulsed laser
spectrum	broad ~ 800 nm	broad ~ 400 nm	discrete lines
pattern effects	not significant	significant, but reduced	significant
operation mode	wafer by wafer	wafer by wafer	wafer scanning

Figure 1. Comparison of important parameters of different short-time annealing techniques; RTA is rapid thermal annealing, and FLA is flash lamp annealing.

using flash lamps and lasers are leading in numerous applications. Due to a short and highly energetic heat pulse, only the near-surface region is annealed, which distinctly reduces the thermal budget on the substrate material. During the short annealing time, the substrate heats up gradually due to thermal diffusion up to a fairly low temperature. This leads to rapid cooling of the surface after annealing. The annealing time can actively control diffusion and electrical activation of impurities, crystallization, and other reordering processes. Moreover, the use of the liquid phase on the short time scale allows for advanced processing. This has led to greater use of fast thermal processing, replacing early chip processing technologies for thin layer engineering of both flexible and rigid substrate materials like glass, plastics, metals, and paper.

In this paper several key applications and equipment issues of short-time annealing are discussed. The focus is on the engineering of thin layers deposited on several substrate materials using flash lamps. More extensive reviews of FLA appear in [12, 13].

EQUIPMENT

The typical setup of an FLA tool in classical semiconductor wafer processing is schematically shown in Figure 2. The wafer is processed in a chamber that is flooded with an inert gas if needed and is supported by a holder made of quartz. A bank of halogen lamps below the wafer are used to preheat the wafer, which is needed to reduce strong-temperature gradients between the back and front sides. This heating takes place in a few seconds and is principally the same process as for RTP. The flash pulse itself is provided by a bank of Xe flash lamps on the front side. The reflector above the flash lamps directs the light toward the wafer and ensures a better homogeneity of the light on the wafer surface. For protection purposes the preheating and flash lamps are separated from the wafer by quartz windows. More details about the basic technical features of FLA equipment and its operation concerns, such as Xenon lamp issues, temperature distribution and measurement problems, strain and stress, and outgassing, as well as reproducibility and homogeneity, are in Ref. [13].

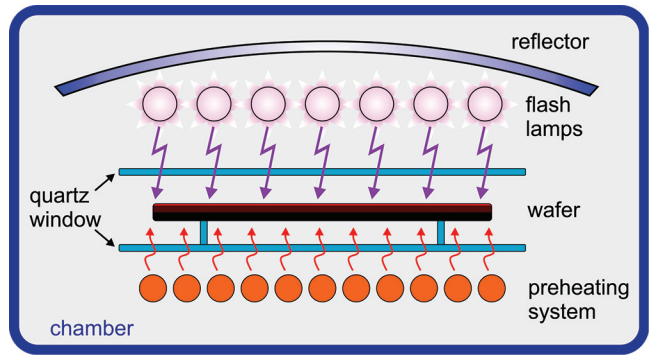

Figure 2. Traditional setup of an FLA tool as used for semiconductor wafer processing.

Recent developments are related to the thermal treatment of flexible or large-area substrates by pulsed annealing (FLA, IPL, or photonic curing). Flexible substrates demand a roll-to-roll transport system and have different requirements of the pulse annealing system. Normally, flexible substrates are processed in larger facilities in a process comprising several steps including deposition, patterning, and annealing. Consequently, the pulse annealing tool is integrated into the processing line as a module (see Figure 3a [14]). Because of heat-sensitive substrate materials the required annealing temperatures are lower than those in the semiconductor industry. On the other hand, higher repetition rates are needed depending on the speed of the roll-to-roll process and the irradiation area of the pulse annealing tool. Depending on the mode of irradiation, pulsed annealing is performed in continuous or camera mode [15]. In continuous mode (Figure 3b), the whole area is annealed, but between two subsequent shots there is a small overlap zone where FLA has been applied twice. If this is not acceptable, FLA is run in camera mode (Figure 3c), where two subsequent shots are separated by a small but untreated stripe.

DOPING OF SEMICONDUCTORS – THE DRIVING FORCE

Doping of semiconductors is an interesting topic. The approach is based on annealing of ion-implantation-induced

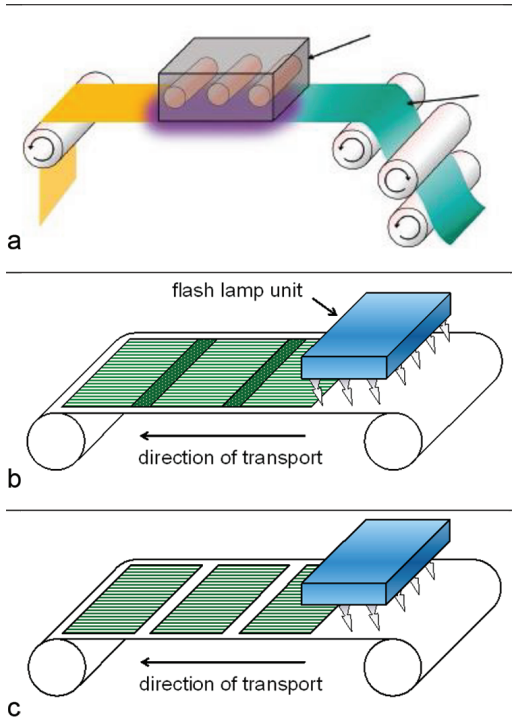

Figure 3. (a) Basic scheme of an FLA tool for roll-to-roll processes, (Copyright 2015 John Wiley and Sons) [14], (b) FLA operation in continuous, and (c) camera mode.

radiation damage. The final goal is the electrical activation of the atoms [6, 8]. The annealing temperature and time actively control dopant diffusion and electrical activation, respectively. Short-time annealing is a necessary prerequisite for shallow junction formation where strongly reduced diffusion without any loss of electrical activation is required. Moreover, advanced complementary metal–oxide–semiconductor (CMOS) device technologies require the formation of ultra-shallow junctions in the source/drain extension regions that play a critical role in device characteristics. The shallow junctions strongly influence the current drive capability and other short-channel effects [16]. An important problem regarding the p-type doping with ion-implanted boron is the well-known effect of transient enhanced diffusion due to silicon interstitial kick-out [17]. This problem can be solved by applying shorter annealing times in combination with higher temperature-time gradients during the heating-up and cooling-down cycles. Pattern effects during chip processing also have to be taken into account; this leads to a variation of optical properties across the patterned wafer surface [18]. A recent review written by Paul Timans on pattern effects of thermal processing includes the aspects of millisecond and laser annealing [19]. It describes specific applications for millisecond annealing during the fabrication of planar and fin field effect transistor (FinFET-style) CMOS transistors [8].

PHOTOVOLTAICS

Doping

The use of FLA was to reduce damage from ion implantation and improve electrical properties. The science community was reluctant to adopt this technology because of the high cost factor, especially with beamline implantation. During the last 10–15 years the interest has increased.

FLA-related activities for photovoltaic applications were driven by two groups. Ohdaira et al. concentrated on the crystallization of amorphous silicon on glass [20–26]. The Rossendorf group used FLA in a broader framework. A new technology with FLA as the key annealing step after doping by ion beam implantation or plasma immersion implantation was developed. FLA was used to simplify the fabrication process of dirty-silicon solar cells, by reducing the number of process steps and cost [27]. In this case an amorphous doped Si layer was the result of an ion beam phosphorus implantation step that replaced the traditional $POCl_3$ doping. In contrast to RTP and furnace annealing, FLA was able to successfully activate the dopants for the required sheet resistance range of solar cells and to suppress the diffusion of metal impurities; this resulted in an increase of the minority carrier diffusion length up to one order of magnitude (i.e., 80 µm without surface passivation). Further improvements were achieved by replacing the conventional ion beam implantation with the cost-effective plasma immersion ion implantation using a phosphine- and hydrogen-containing plasma [28]. In this study the influence of FLA parameters, the hydrogen content of the annealing ambient, and its effect on the minority carrier diffusion length were investigated in detail.

Normann et al. [29] and Riise et al. [30] investigated the vertical diffusion of phosphorus and boron using spin-on deposition of a phosphorus and boron source, respectively, on the surface of monocrystalline silicon wafers. This was followed by FLA as a method to form high-concentration shallow emitters for solar cells. By varying both the energy density of a 20 ms FLA step in the range from 62 to 132 Jcm^{-2} and the sample preheating, it was observed that FLA treatments can diffuse a high concentration of phosphorus atoms that are electrically active. The most promising P-emitters were obtained after FLA in the energy range from 110 to 128 Jcm-2 including preheating at 300°C with a phosphorus concentration of $4–6 \times 10^{20}$ cm^{-3}. The emitter junction depth after these treatments is in the range of 100–200 nm. Sheet resistance values in the range of 60–100 Ohm/sq. were reached for both dopant types. For boron, optimum emitters were reached for energy densities below 105 Jcm-2

for 10 or 20 ms annealing time leading to an emitter junction depth below 150 nm. For the boron case no preheating was needed. Like the well-known case of boron implants a transient enhanced diffusion effect was observed [17]. Here, the effect was explained by Si interstitial injection originating from a thermally activated reaction between the spin-on diffusant film and the silicon surface.

Thin Silicon Films on Glass

Crystallization of thin silicon layers has been worked on over many years, resulting in annealing times ranging from seconds to nanoseconds, for flat-panel active matrix liquid crystal displays. To realize low-cost large-area wafers the polycrystalline silicon is generally grown on cheap glass substrates. This is the same requirement for photovoltaic applications because the cost factor is even more stringent. A key requirement of the processing conditions is for temperatures of the glass not to exceed its softening point, which is around 600°C for low-cost glass [31]. There are several established methods of film preparation that are compatible with this constraint on processing temperature. These are direct deposition of polycrystalline silicon and solid phase crystallization or laser crystallization of amorphous silicon. The development of the explosive crystallization, as well as the chance of operating in the liquid phase regime, opened fascinating processes for materials modification. For more detailed information about this topic, see Ref. [13].

Pioneering work by Pecz et al. [32] and Smith et al. [33] introduced the FLA application for this material in 2005. They investigated and modeled the crystallization of amorphous silicon (a-Si) layers by FLA. Intrinsic a-Si films with thicknesses of 50–250 nm were deposited on glass and crystallized by FLA under different energy densities with a flash duration of 20 ms. Two different glass substrates were used for the deposition of a-Si films, Corning Code (CC) 7059 and CC 1737. Then a 100-nm-thick SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) as a protection layer on the glass, before the deposition of the a-Si film. The a-Si films were deposited by low-pressure chemical vapor deposition (LPCVD) at 420°C, using disilane. They crystallized by forming grains with a mean size up to 6 mm, almost free of ingrain defects. As for the case of excimer laser processing, solid phase crystallization and super lateral growth were noted as growth mechanisms. It was also demonstrated that FLA successfully eliminated the in-grain defects in poly-Si films already crystallized by conventional low-temperature furnace annealing [32]. The model by Smith et al. included both the thermal response of the wafers and the phase transition scenarios. Predictions from the model correlate well with existing experimental data, and the model can be used to optimize process conditions [33]. Ohdaira et al. investigated several aspects of the crystallization of amorphous Si layers with thicknesses in the μm range for photovoltaic applications in studies that included the influence of different substrates [21] and different deposition techniques [23, 26].

The Korean group devoted most of their activities to FLA of amorphous silicon layers on 500 μm thick glass substrates for display technology [34–38]. The following layer stack was arranged on top of glass: 0.03 μm silicon nitride plus 0.3 μm silicon oxide plus 0.07 μm of amorphous silicon, all deposited by PECVD. Aspects of boron and phosphorus doping as well as thermal warpage of the glass substrates and issues of scanning multi-shot irradiations were investigated. Of special interest are the considerations about the warpage of glass under FLA, which continued earlier work by Smith et al. devoted to silicon wafer substrates [39].

One important issue for photovoltaics is hydrogen handling, as on one side a low hydrogen content is desired in order to avoid crack formation or delamination during FLA, whereas on the other side hydrogen passivation is needed to achieve long minority carrier lifetime; see the paper of Bregolin et al. for the case of doping photovoltaic silicon [28]. Ohdaira et al. [22] reported that the surface region of about 500 nm of a 4.5 μm thick film of a-Si deposited by catalytic CVD was rich in defects and voids after annealing by FLA using a 5 ms flash pulse. Minority carrier lifetimes below 10 μs were measured even after removing this surface region. The lifetime values improved after a subsequent high-pressure vapor anneal, but the best properties were obtained after an additional post-FLA processing step, namely conventional furnace annealing at 450°C (see Figure 4). The sharp increase in lifetime is explained by the enhanced dissociation of hydrogen molecules leading to the appropriate termination of dangling bonds. In contrast, the large decrease in higher annealing temperatures is explained by the unwanted dissociation of Si-H bonds and out-diffusion of hydrogen.

Copper Indium Gallium Diselenide (CIGS)

A novel process for the formation of copper indium gallium diselenide (CIGS) films was proposed by Dhage et al. [40, 41]. CIGS films with a thickness of 4 microns and grain sizes from 0.3 to 1 microns were prepared from a Cu(In0.7Ga0.3) (CIG) metallic alloy and Se nanoparticles by the IPL technique. The melting of the CIG and Se nanoparticles and the nucleation of CIGS occurred in a very short reaction time of 2 ms. It is assumed that the Se diffuses into the CIG lattice

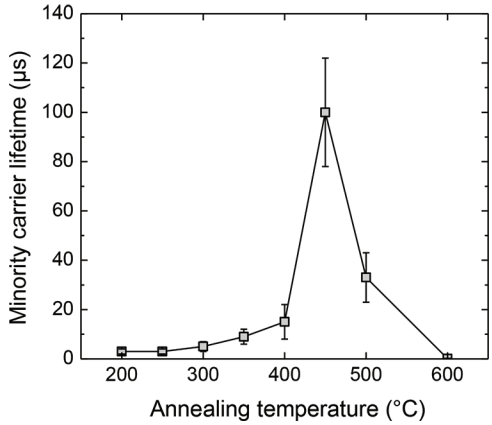

Figure 4. Minority carrier lifetime of a polycrystalline Si film as a function of the annealing temperature of post-FLA furnace annealing with an annealing time of 30 min in N_2 ambient. Data taken from [22].

to form the CIGS chalcopyrite crystal structure. This experiment was performed on conventional glass plates; another study recently reported on IPLtreated CIGSlayers on flexible glass [42].

Another photovoltaic application of FLA was performed by Seeger et al. [43] and Reck et al. [44] for the improvement of the optical properties of copper–indium–(gallium)–sulphide films (CI(G)Su) and related chalcopyrites using zinc oxide films and FLA. The goal was the modification of the surface at the $Cu(In,Ga)S_2$-CdS interface by preparing a shallow zinc profile without doping the whole absorber layer. Polycrystalline layers of such compound semiconductor materials with band gap energies well matched to the solar spectrum make suitable absorber layers for thin film solar cells [43].

TRANSPARENT CONDUCTIVE OXIDES (ITO, ZNO, AZO)

Dielectric or insulating layers were also part of the activities to use FLA as an advanced tool for new technological approaches. One of the first activities was related to the ion beam synthesis of silicon dioxide by high dose oxygen implantation. Infrared spectroscopy was used to check the quality of the silicon oxide by observing the Si-O stretching band (wavenumber 1075 cm^{-1}). If a millisecond anneal step could create a similar Si-O quality compared to a high-quality method of thermal oxidation, then FLA could be used for making microelectronic gate oxides and other oxides. Hensel et al. reported a successful FLA experiment in 1985 [45] showing that the ideal wavenumber was reached for a layer with a stoichiometric oxygen dose by using an energy density of 84 J/cm^2 and a pulse time of 10 ms. In recent years high-k dielectrics of the so-called second generation ($LaLuO_3$ and $LaScO_3$) were treated with FLA to avoid detrimental crystallization effects [46].

The transparent conductive oxides (TCO) and inkjet-printed films are of much higher interest as functional thin layer coatings for photovoltaics and low-cost electronics.

Indium Tin Oxide (ITO)

ITO modification by FLA was demonstrated about ten years ago at the rapid thermal processing (RTP) conferences [15, 47]. The main goal was the maximum resistivity decrease of t with highest visible transmittance as is usually required for ITO layers. The resistance of inkjet-deposited layers was decreased by about two orders of magnitude with just one flash. If there is too much energy introduced the layers will crack on a microscopic scale (see Figure 5). This led to an increase of the resistance.

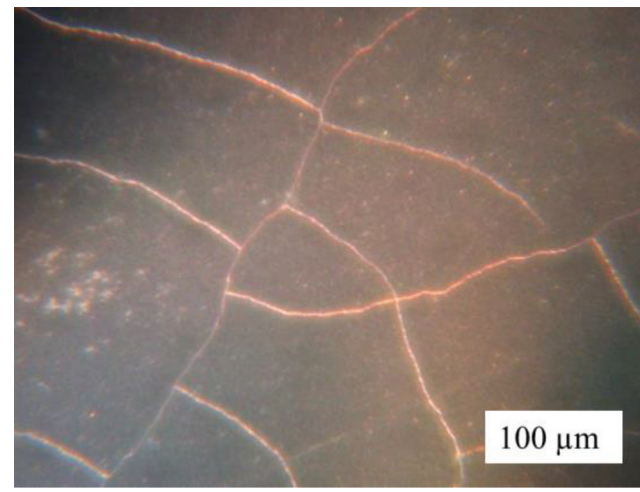

Figure 5. ITO layer with cracks on PET plastic foil taken with a light microscope.

In order to ensure high-quality TCO layer formation the deposition process has to be performed at a temperature higher than the recrystallization temperature. High deposition temperatures limit the number of possible substrates where the TCO could be used. Weller and Junghähnel demonstrated highly conductive crystalline ITO on ultra-thin glass using FLA to recrystallize the deposited ITO layer [14]. Glass substrates thinner than 200 µm are flexible and allow for the use of roll-to-roll processing.

Temperature distribution modeling for ITO-on-PET [15] and ITO-on-glass are shown in Figure 6. Figure 6 shows the simulated temperature distributions for 150 nm ITO on a 100-µm glass foil for different depth regions and different

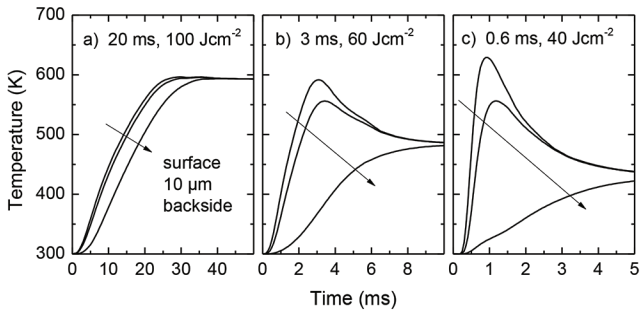

Figure 6. Temperature distribution in the system ITO glass (150 nm thick ITO layer on a 100 µm thick glass foil) for different flash pulses. The depth indications are related to the surface.

pulse durations. In the case of 20-ms annealing time there is little difference between the front and back sides of the foil, but as the pulse duration shortens, this difference becomes larger. In addition, the energy density of the flash pulse necessary to achieve a certain surface temperature decreases. Thus, flash pulses shorter than 1 ms are especially suitable for flexible substrates. Furthermore, the present case of a transparent film on a transparent substrate is challenging as only the UV part of the flash lamp spectrum can be utilized. The temperature trends in Figure 6 are generally valid, but the specific energy density values are an overestimation. At first, the ITO literature values used for optical absorption leads to an absorption of less than 5 % in the ITO layer. Second, reflections at the chamber walls were not considered. Thus, in practical experiments as performed in [14] similar temperature profiles can be achieved with significantly lower energy densities.

Extensive work for FLA at ITO on glass backplanes was also done by Kim [48] using 0.4 ms flashes for 100-nm-thick ITO layers on 500-micron-thick glass reaching similar resistivity values as in the case of glass foils [14]. Recently, Scherg-Kurmes et al. have shown that an FLA treatment for 2.7 ms of amorphous hydrogenated indium oxide (In_2O_3:H) leads to recrystallization independent of the substrate temperature during the deposition [49]. The recrystallized In_2O_3:H layer was polycrystalline with a carrier mobility higher than 100 cm^2/Vs, which is comparable to a thermal anneal at about 180°C for 15 min.

ZnO

Gebel et al. [50] published results of FLA on zinc oxide layers. ZnO:Al films with a thickness of about 880 nm were deposited by magnetron sputtering. The glass substrate was not heated, neither before, during, nor after the deposition. Subsequently the deposited layers were treated by FLA at 1.3 ms. Using this method, the resistivity of the ZnO:Al films decreased by a factor of two, down to 1.0×10^{-3} Ohm-cm.

The microstructure revealed by cross-sectional transmission electron microscopy (XTEM) showed a typical preferred orientation of the c-axis perpendicular to the substrate surface, which is known for TCO layer growth (Figure 7). There was basically no visible difference between the microstructure and the thickness of the as-deposited and the FLA-treated layers.

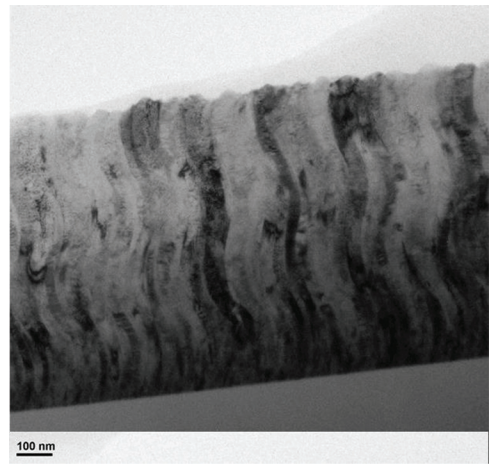

Figure 7. XTEM micrograph of an FLA-annealed AZO layer, after Gebel et al. [50]

These results were in agreement with those reported from rapid thermal processing or furnace annealing treatments. Despite the very short annealing time of only 1.3 ms the resistivity and transmittance in the UV and the blue spectral ranges were considerably improved. Figure 8 demonstrates the results of calculations showing the band gap shift after FLA treatment.

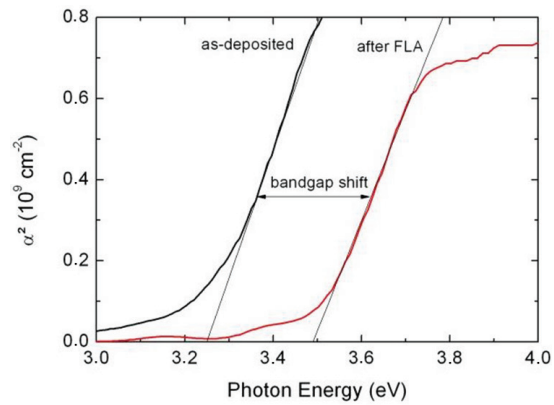

Figure 8. Optical band gap calculation for as-deposited and annealed (7.5 Jcm^{-2}) AZO layers, after Gebel et al. [50].

In another approach, plasma-assisted reactive pulsed-laser deposition followed by plasma immersion ion implantation of SF_6 and post-implantation, millisecond FLA was used to fabricate nanocrystalline, highly n-type ZnO films on silicon wafers with superior properties [51]. The n-type doping was realized by the incorporation of F into the oxygen lattice site of ZnO and the efficient passivation of dangling bonds at grain boundaries. It was shown that during the FLA (35–50 J cm^{-2}) the fluorine was electrically activated and the current-voltage characteristics revealed rectifying transport properties in the n++-ZnO:F/n-Si structure. The fluorine doping reduced the concentration of optically active defect centers. After annealing, the ZnO films were fully recrystallized, and maximum photoluminescence emission was obtained after annealing at 40 Jcm^{-2} for 20 ms. Annealing at higher energy led to the degradation of film crystallinity and to a decrease of the photoluminescence emission.

The effect of millisecond FLA on aluminum-doped ZnO (AZO) films and their interface with a silicon wafer surface was also investigated [52]. The AZO films were deposited by magnetron sputtering on Si (100) substrates. The resistivity of the AZO film was reduced to a level close to state-of-the-art value of 2×10^{-4} Ohm-cm after FLA for 3 ms with an average energy density of 29 J/cm^2. Most of the interfacial defect energy levels were simultaneously annealed out, except for one persisting shallow level, tentatively assigned to the vacancy-oxygen complex in Si, not affected by FLA. Subsequent to the FLA, the samples were treated in N_2 or forming gas (N_2/H_2, 90/10) atmosphere at 200–500°C. These latter samples maintained their low resistivity values achieved after the FLA but not the former ones. The interfacial defect level persisted after the FLA treatment was removed by the forming gas treatment, at the same time as another level emerged at ~0.18 eV below the conduction band. The electrical data of the AZO films were correlated to point defects controlling the resistivity. It seemed that the FLA promoted the formation of electrically neutral clusters of zinc vacancies (V_{Zn}) rather than passivating/compensating complexes between the Al donors and V_{Zn}. Impurity profiles of the interfacial region obtained by secondary ion mass spectrometry showed that there existed sensitive dependencies on the FLA energy density (see Figure 9).

The dominating impurities in the AZO films were Al and H, homogenously distributed to a depth of ~140 nm (see Figure 9). The H content was in the range of 10^{18} cm^{-3}, about two orders of magnitude below that of Al. Al appeared as the clearly dominating shallow donor impurity. All other elements were estimated to be in the range of 10^{17} cm^{-3} or below.

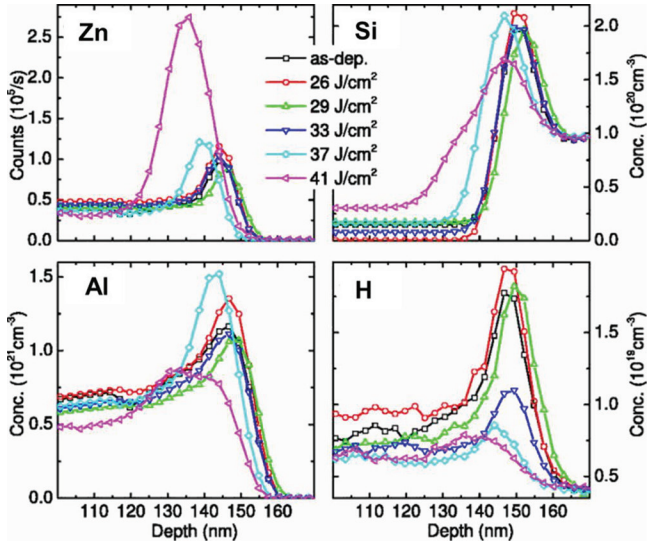

Figure 9. Depth profiles of Zn, Si, Al, and H determined by secondary ion mass spectrometry after FLA treatments using different energy density. Reprinted from [52] with the permission of AIP Publishing.

The interfacial redistribution started for energy densities above ~37 J/cm^2, causing a silicon in-diffusion into the AZO layer (Figure 9, Si part). Comparable effects were seen for oxygen (not shown), Al, and Zn. This demonstrated a broadening of the interfacial region. At the same time, the amount of hydrogen decreased.

FLEXIBLE ELECTRONICS AND INK JET PRINTING

Novel, flexible, and low-cost electronic products with a functionality far beyond the conventional size-restricted and rigid semiconductor devices require a rapid development of advanced material and preparation technology concepts. One of the most promising approaches to realize this ambitious goal is printed, flexible, and stretchable electronics (PFSE). A recent review was presented by Sigurd Wagner, one of the pioneers in this field. He wrote, "Stretchable electronics is the newest class of large-area electronics. Quite literally large-area electronics has become a success story: flat panel displays are manufactured at the rate of 100 and solar cells at 200 square kilometers a year. Many of these products are made with thin films. Liquid-crystal displays are driven by active matrices of amorphous silicon transistors, 2 and 10 % of all solar cells are made of amorphous silicon and chalcogenide films, respectively. Like any other stiff material, circuits become flexible and rollable when their thickness is reduced to 1/1000 of the desired radius of curvature. Thin film circuits are made on flat surfaces by standard microfabrication techniques. When made

on plastic substrates and with plastically deformable interconnects, they can be shaped to surfaces that need expansion out of the plane" of the film, "for instance spherical caps. On plastic substrates, this deformation is permanent. Elastomeric substrates and elastic interconnects" allow circuits to have freedom of shape "to reversible deformation and near-arbitrary dimensions. Sizes and shapes of elastomeric circuits can be changed reversibly by applying mechanical force, by gas pressure, or by application of an electric field" [53].

After 2006, the Rossendorf group was successfully using millisecond thermal processing by FLA as a highly-attractive technique for the functionalization of ITO layers on glass and PET [15, 47] as well as of copper and silver paste screen printed on low-thermal budget paper-like media for package labeling [unpublished results]. The effect of the FLA parameters (pulse duration, energy density) on the substrate behavior as well as on the microstructure and electrical response of the as-flashed films was studied. A significant drop of the sheet resistance of the FLA-treated layers as compared to the as-printed layers was observed. As FLA permits selective, near-surface heating, damage of the sensitive substrates was avoided. The microstructure of the copper paste before and after FLA was also investigated. In Figure 10, the correlation between the achieved sheet resistance values and the corresponding microstructure of the copper paste films is presented.

More activities to use short-time annealing after inkjet printing started in 2009 with a paper by Kim et al. [9]. Nittynen et al. recently compared FLA with laser annealing

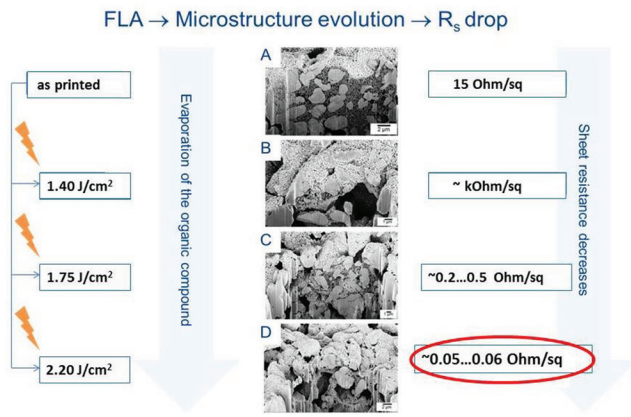

Figure 10. Illustration of the relation between the applied annealing conditions, evolution of the samples microstructure and resulting sheet resistance. Material studied: Cu-film/PET, No. 3. (a) Virgin material, (b) as-flashed, E_D = 1.4 J/cm², (c) as-flashed, E_D = 1.75 J/cm², and (d) as-flashed, E_D = 2.2 J/cm². The pulse time was 600 microseconds.

(diode laser 808 nm) for inkjet-printed copper nanoparticle layers [54]. A conductivity of more than 20 % of bulk copper was obtained with both sintering methods. Both methods are complementary techniques and highly suitable for this application field. A good source of new information is the NIP & Digital Fabrication Conference [55]. Printing has successfully demonstrated its potential for manufacture of advanced low-cost products (e.g., flexible displays, thin-film solar cells, and large-area sensors). By using bendable, inexpensive media (e.g., paper-like substrates, polymer films) and high-throughput roll-to-roll processing, a significant reduction of the overall costs was achieved.

It was demonstrated by Yung et al. [56] that even a commercial camera flash device (in this case Nikon Speedlight SB-22) can be used for sintering of inkjet-printed silver tracks on polyimide, polyethylene terephthalate, and photographic paper at room temperature. In this case the enhanced photothermal effect in silver nanoparticles was used.

Being highly efficient (ultra-short), "non-destructive" (suitable for low-thermal tolerance flexible media), and compatible with roll-to-roll processing, FLA offered the realization of advanced PFSE products.

CONCLUDING REMARKS

Although the basic effects regarding the use of energetic light pulses (lasers, flash lamps) were already explored in the mid-1970s, the real industrial applications started after 2000 in advanced chip technology for engineering ultra-shallow junctions on silicon wafers. Meanwhile new fields of application were developed using the main advantage of short energetic pulses in the time range of several milliseconds or less. Low-cost electronics based on substrate materials like plastic foil, thin glass, cardboard, and paper drove performance issues for equipment and processing. A number of convincing results were reported during the last years and were commented in this paper. TCO layers, inkjet-printed patterns on such substrates, and short time annealing approaches need further attention from the R&D community.

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FOR MORE INFORMATION:

Wolfgang Skorupa, Institute of Ion Beam Physics and Materials Research, Postfach 51 01 19, Bautzner Landstrasse 400, 01314 Dresden, Germany, w.skorupa@hzdr.de, 9/351 260 - 3612